From Nuts to Nodes, along the game trail

Integrating and verifying the complexity and diversity of lithographic manufacturing

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Veldhoven

ASML and Confidence in diversity: setting the scene

ASML creates semiconductor manufacturing equipment supported by process solutions.

60 offices in 16 countries, 35000 employees from over 130 nationalities

ASML as system integrator works with a wide array of advanced suppliers

Amongst those TNO-ESI: congratulations on your 20th birthday!

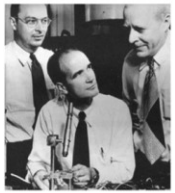
ASML and Confidence in diversity: it is people that make it happen.

To tackle technical diversity, we have to tap the strength of human diversity

A short history of the Integrated circuit

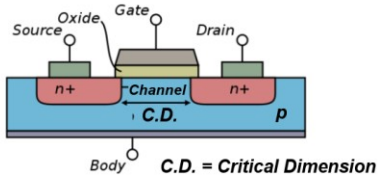
Integrated circuits of transistors / MOSFETs, invented at AT&T Bell labs
Bardeen, Shockley, Brattain Nobel Prize 1956

First build transistor, 1948
(Germanium based)



Left to right:
Bardeen,
Shockley,
Brattain

Mohamed Atalla
and Dawon
Kahng



MOSFET, 1959
Metal Oxide Semiconductor
Field Effect Transistor

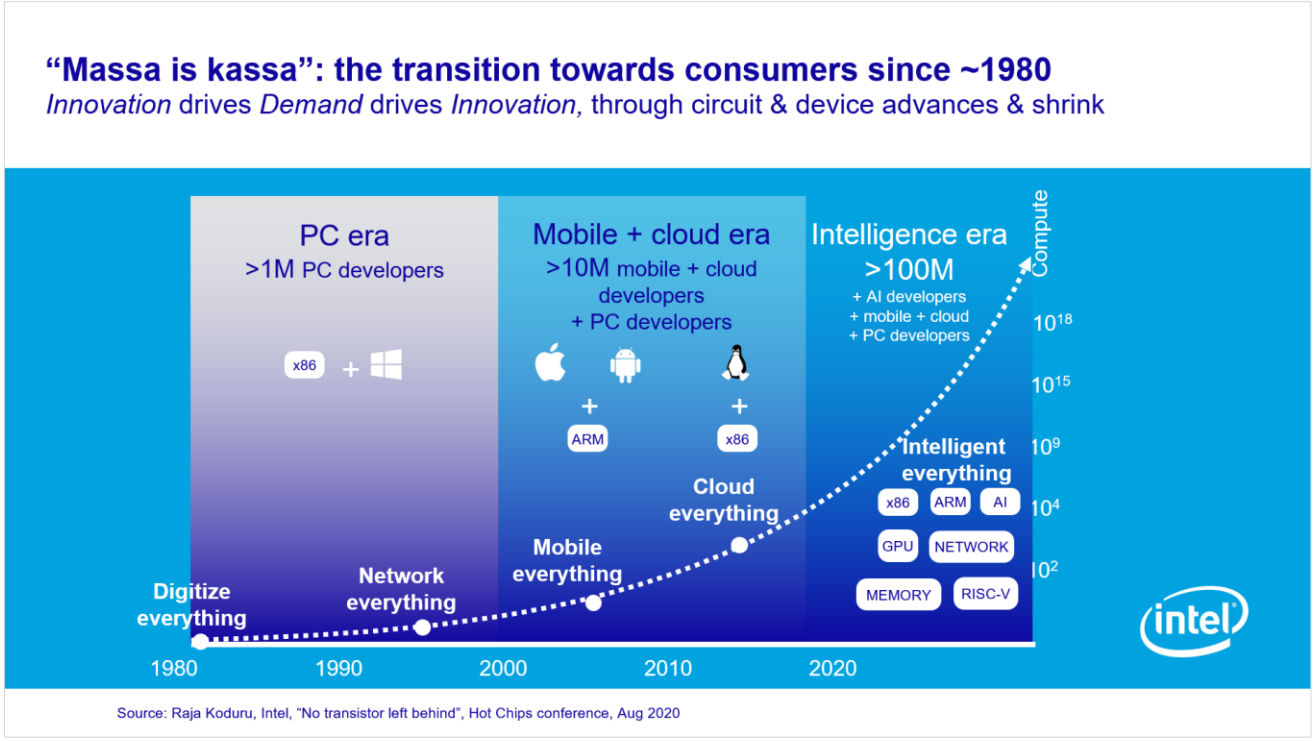
Moore's Law (1965): cost per function halves every other year ('a node')

…, 2, 4, 8, 16, 32, 64, 128 GB…

Predicted home computers, cloud, self driving cars, mobile phones, …

Moore's law drives *Innovation* drives *Demand* drives *Innovation* …

Diversity in integrated circuits and their applications

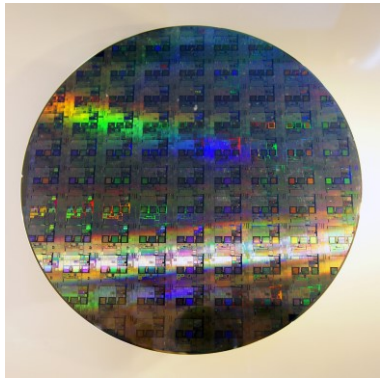


- Circuit: changes in the architecture of chip layout
  - Chip manufacturers
- Device advances and materials:
  - Resist and material suppliers
- Shrink: reducing the size of the features
  - Reticles and scanner manufacturers
  - Metrology equipment

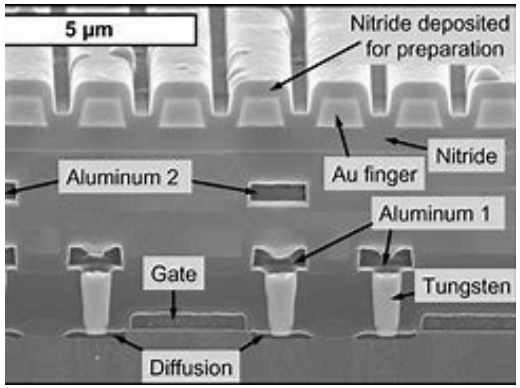
Mosfet on silicon: the crucial role of lithography

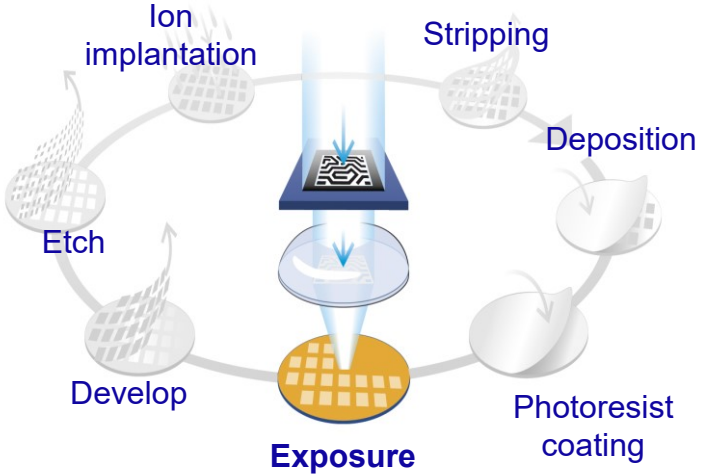
Through circuit & device advances & shrink

5G chip, 2021
12 Billion transistors
@15*15 mm



- Many chips from one 300 mm silicon wafer
- Each chips contains many layers





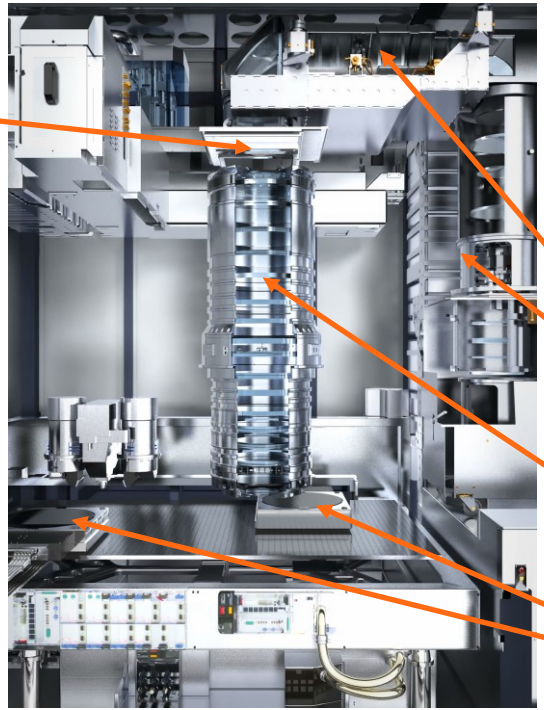
Cycle repeated at least once per layer, up to 60 process steps for a layer.
(Up to ~180 layers per chip)

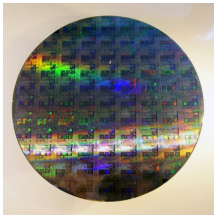
Imaging – Overlay - Throughput

Shrink with (ASML's) wafer scanners: giant copying machines

Exposure is done to pattern circuitry on silicon

Reticle





$CD_{min} = k_1 \cdot \lambda/NA$ (*)

(*) Abbe (1873, Co-founder of Zeiss Optical Works) & Lord Rayleigh
https://www.asml.com/en/technology/lithography-principles

Illuminator and lightsource at wavelength λ

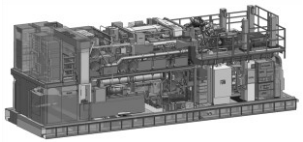
Lens (Numerical Aperture NA)

Silicon wafers on dual stages

CD = $k_1 \cdot \lambda/NA$:
λ, NA and increasing pupil complexity (k_1) determine ASML product roadmap



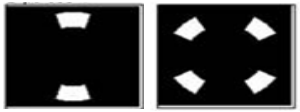
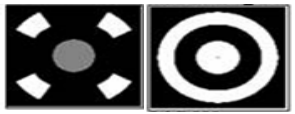
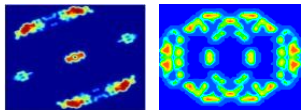


	PAS5500/200	XT:8x0	XT/1100	NXT:1400 – XT:2050i	NXE:3x00	EXE:5x00
λ, NA:	365 nm, 0.6	248 nm, 0.8	193 nm, 0.75	193 nm, 0.95-1.35 (Introduction of immersion lithography)	13 nm, 0.25 (X=3,4,6,8)	13 nm, 0.55

early 90's | *2000* | *2005 – 2008* | *2009 – 2021* | *2012 - 2022* | *2023 -*

k_1

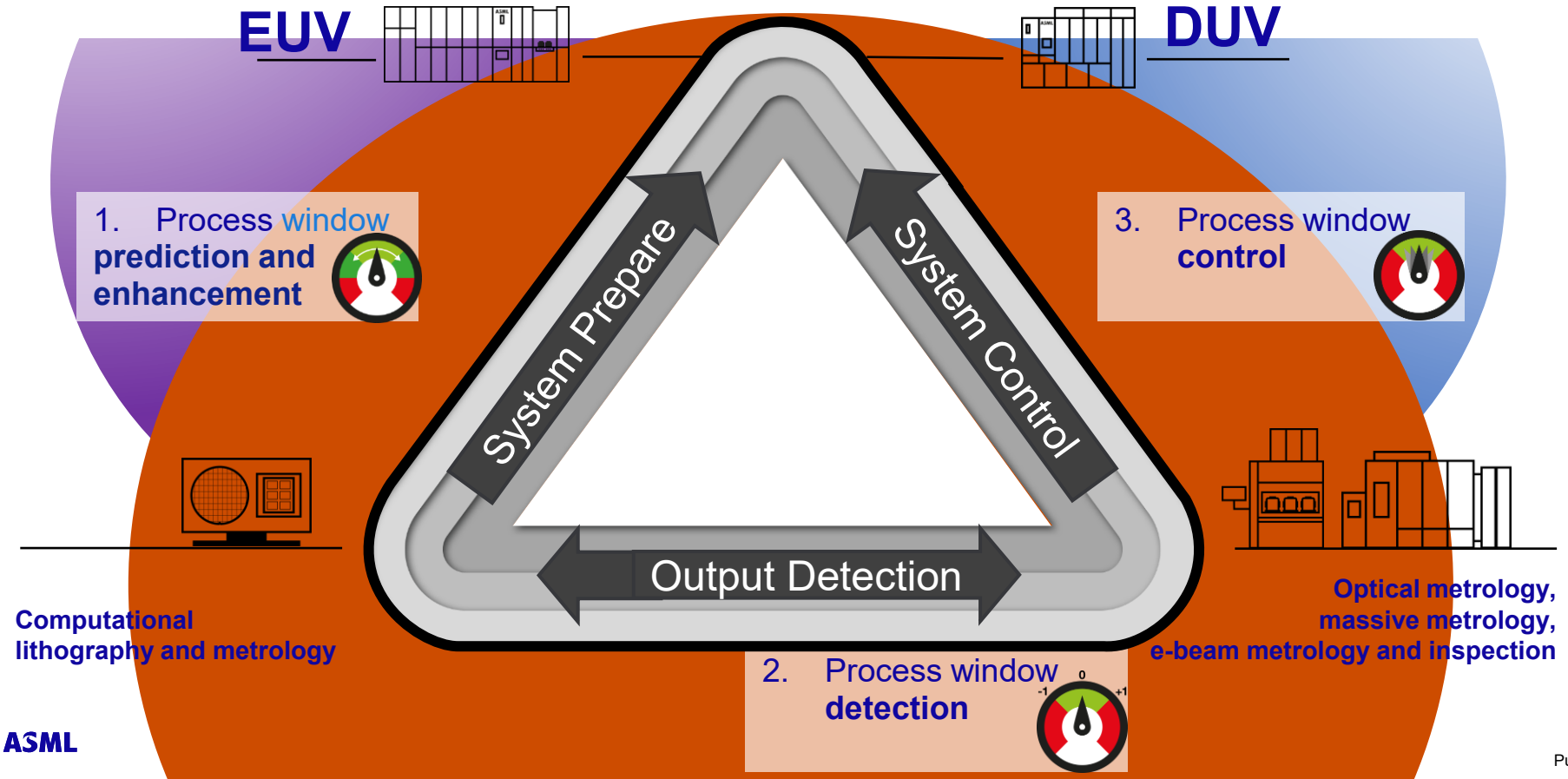





Resists, reticles (masks), Machine learning,

Aerial illuminator | DOE | DOE | DOE | FlexRay

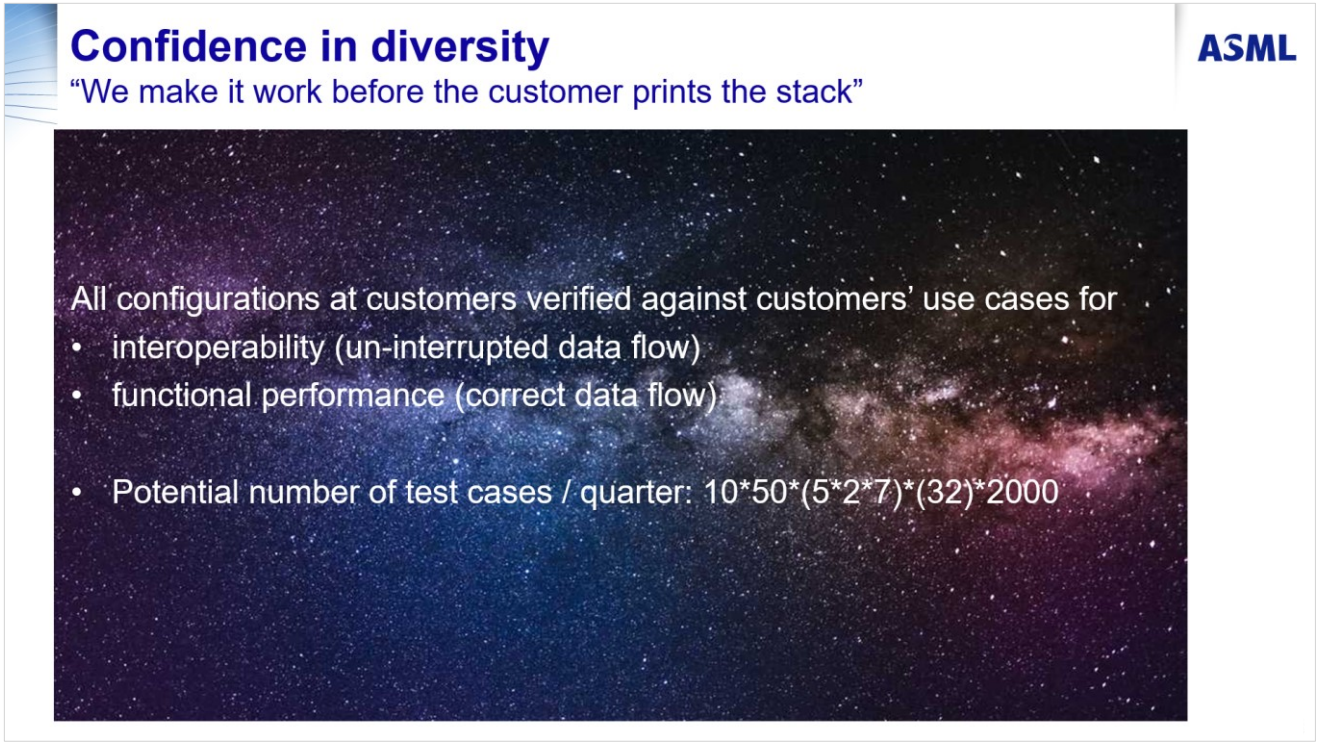
Source Mask Optimization

ASML: “Lithography exposure is supported by process solutions.”



Quantifying the diversity of *holistic* lithography

Over 2 billion test cases per quarter: hence verify early, limited & fast



Focusing on completed individual products into holistic solution

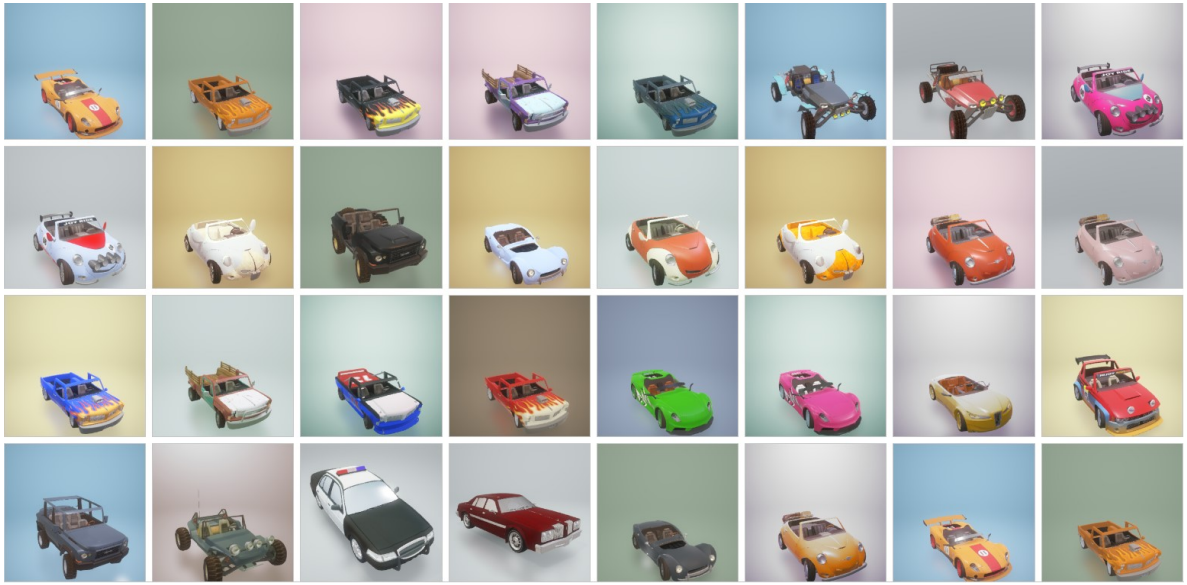
Diversity with 1 patch per quarter

Verify:

- Early
- Limited
- Fast

Verify Early: Functional Clusters

Parallel product development enabled by a functional breakdown

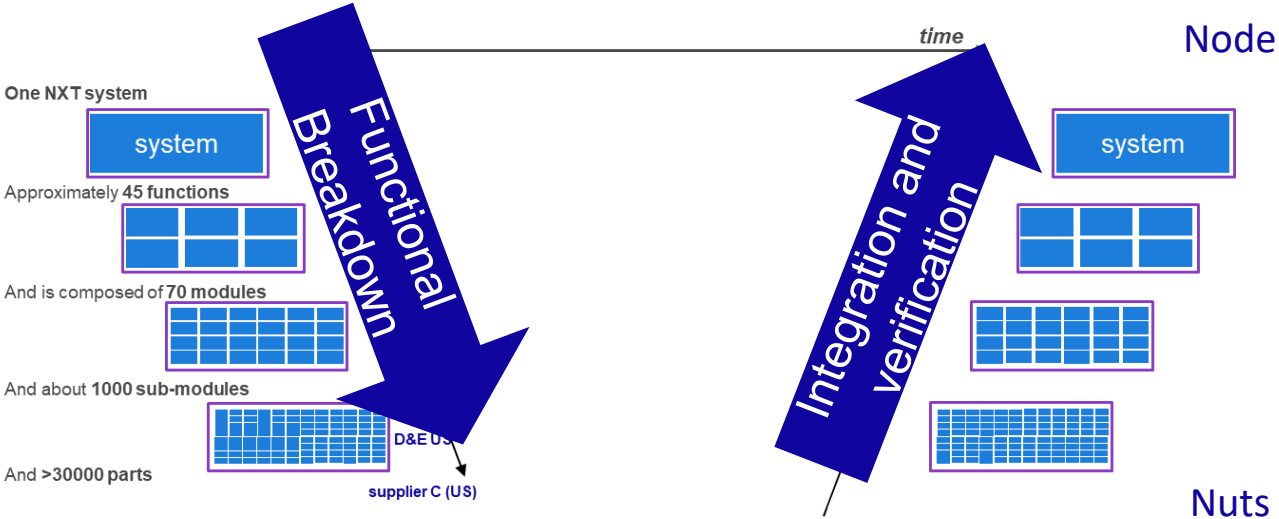


Every civil car needs to

- Be safe
  - Lights, mirror, safety belt
- Move
  - an engine, wheels, steering wheel
- Have a l ook
  - Body, upholstery
- Entertainment
- …

Verify Early: Functional Clusters

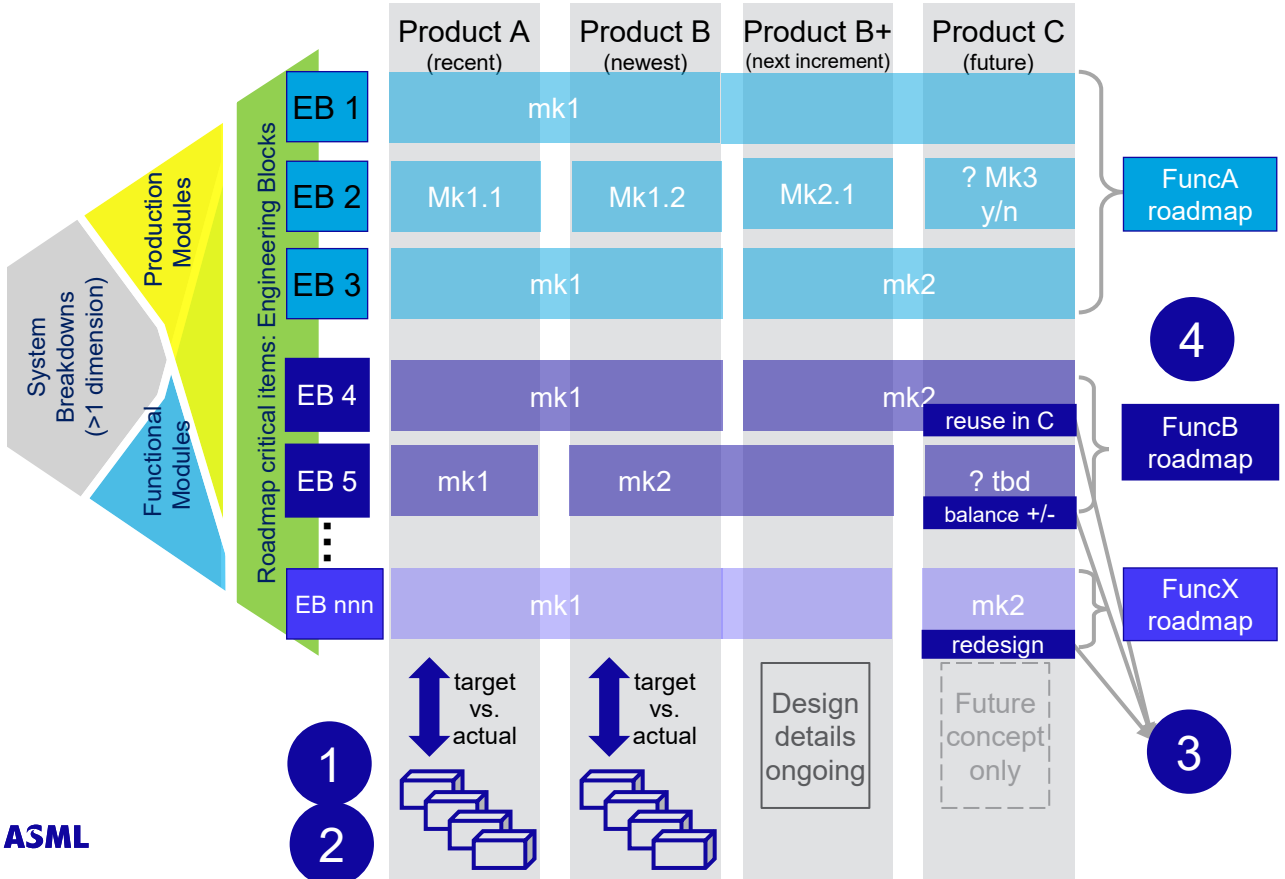
Parallel product development enabled by a functional breakdown of individual systems



- Likewise ASML products
  - Imaging
    - Projection, Illumination, Source, reticles, resist…
  - Wafer handling
    - Stages, handler, load lock
  - Overlay
    - Alignment, sensors, clamps, …
  - SW architecture
    - Computer Systems, Motion Control, Diagnostic …
  - …
- Functional breakdown ownership *at name level*
- With incoming-outgoing specifications established
- From the lowest level component to the holistic solution for the node

Verify Early: Integrating all the parts together into products

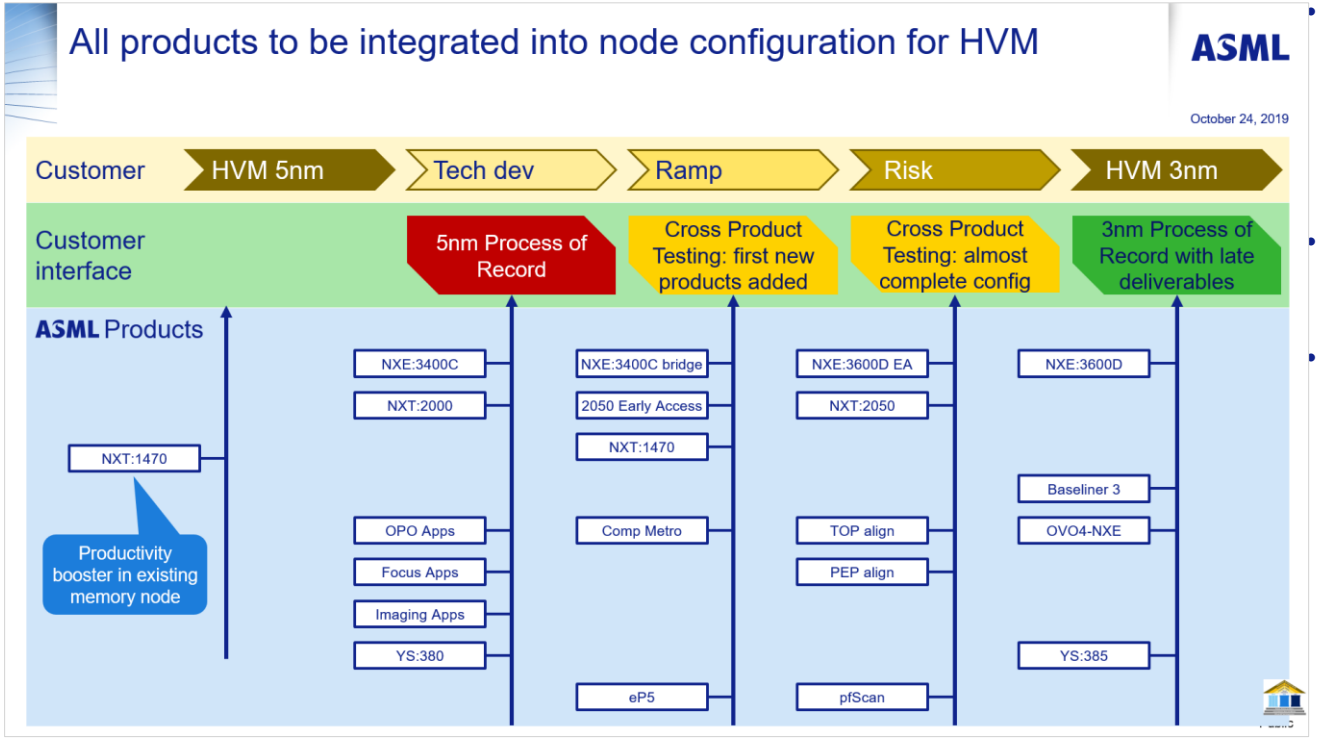
Configuration management at product level for many systems



1. Use engineering blocks to define validated (allowed) system configurations.
2. Engineering blocks only through testing released for integration.
3. Cross-product reuse analysis, incl. performance benefit vs. cost balance of keeping things common.
4. Roadmapping towards future needs (typically per function)

Verify Early: Parallel product development via Node release to customers

Configuration management at node level



- Improve customer time to yield and HVM with verified holistic node solutions fulfilling customers' patterning needs
- Customers are in their own development process
- Verify individual products as well as combinations as used by customers in their manufacturing flow

→What is a customers going to print?
→How is he going to do this?

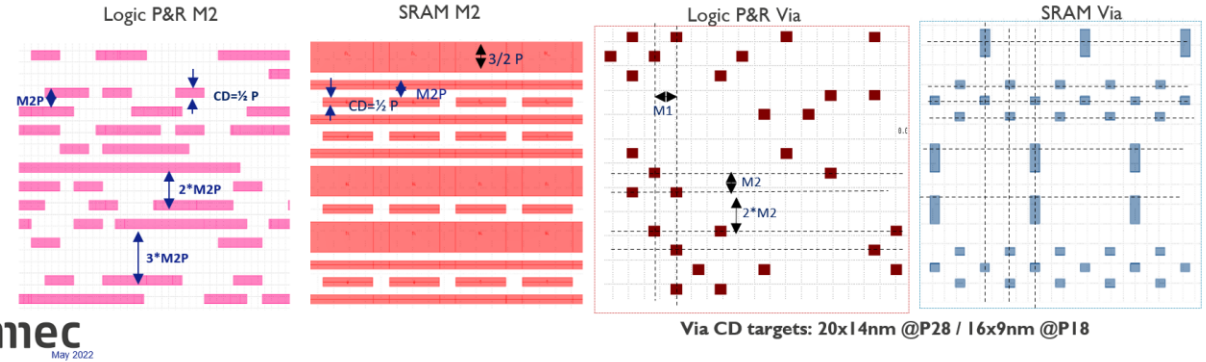
Verify Limited: input from internal and external partners

Design and Verify against real customer use cases …

Representative customer use cases

	Design M2 Pitch	P30	P28	P26	P24	P22	P20	P18
0.33NA	Single Patterning	X	X	X	X			
	Double Patterning			X	X	X	X	X
High NA	Single Patterning	X	X	X	X	X	X	X

M2/M0 and Via Design Details through pitch



Via CD targets: 20x14nm @P28 / 16x9nm @P18

"Clean out the minefield along the game trail."

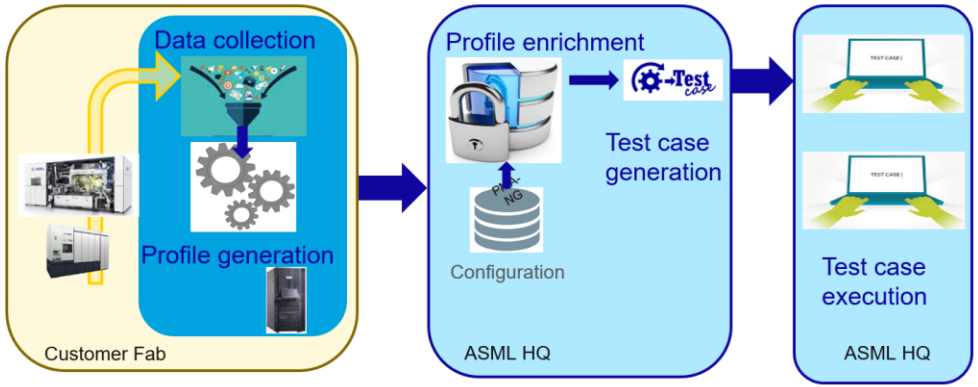
(after Leon Verstappen)

Verify Limited: learning directly from customer's system use

Verify against real customer use cases and customer workflow

Automatically collecting customer workflow through Customer profiling

Requires upfront intimate collaboration with customers to ensure IP protection



"Clean out the minefield along the game trail."

(after Leon Verstappen)

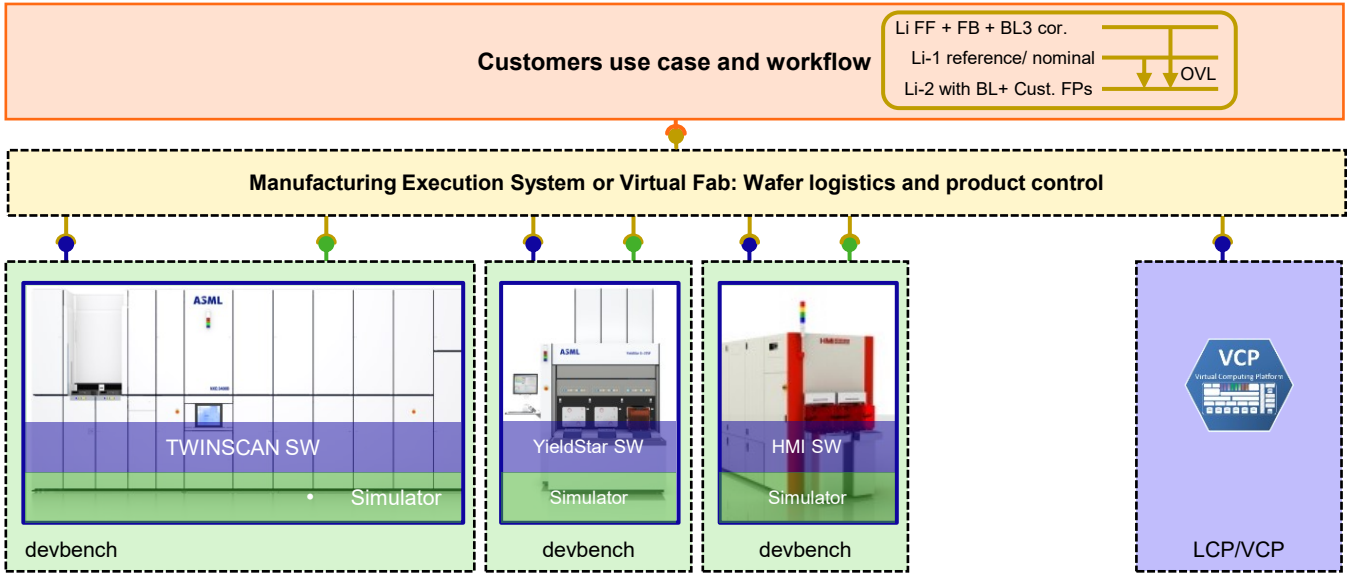
Test design and test methodology in collaboration with TNO-ESI

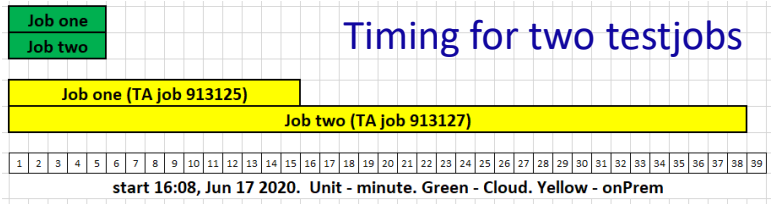
See contribution by Debjyoti Bera

See demo/poster:
Virtual Fab: virtual verification of ASML's holistic lithography solutions
Authors: Karine de Pinho Peralta, Rick Smetsers, Paul van Gorp

Verify Fast through digital and cloud capability

Ensuring an *un-interrupted* data flow across products





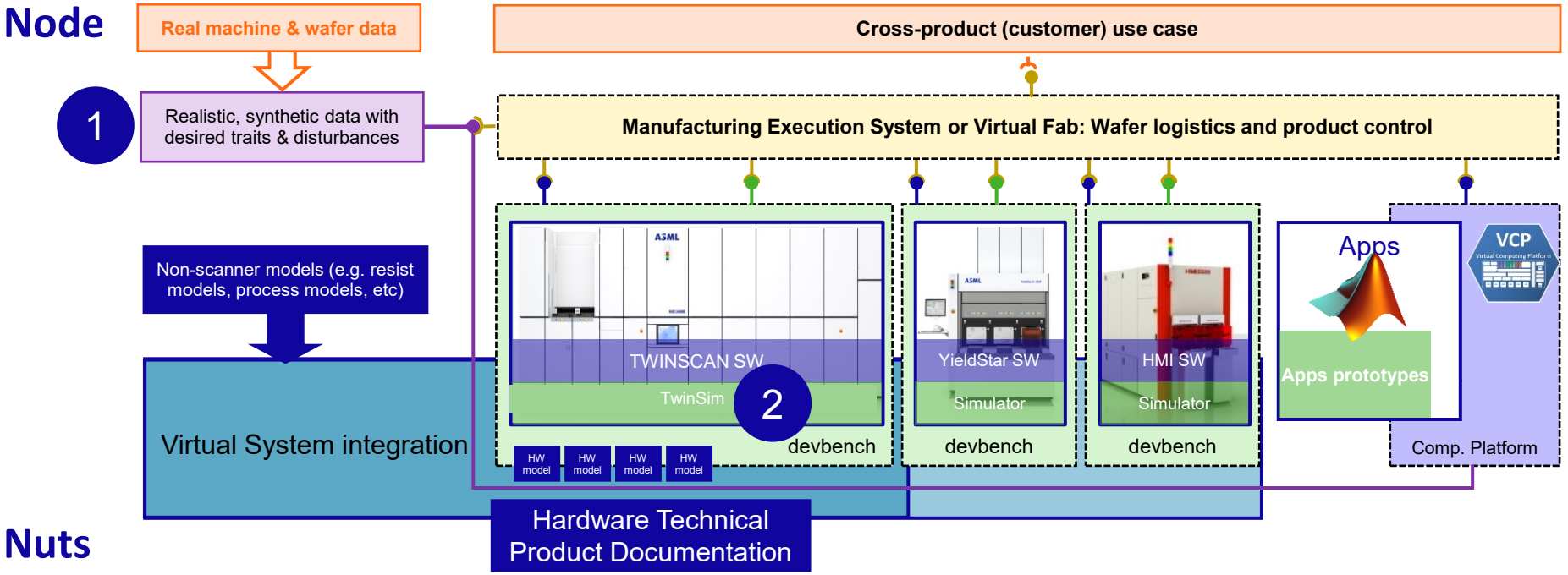
ASML Cloud 10 OnPrem 43

- Verifying digitally
  - Based on real product SW
  - Making use of industry standard interface
  - With Virtual fab representing customers MES (*)
  - (Cheap, too!)
- Verifying in the Cloud
  - 'Unlimited' CPU capacity, on demand
  - Allows mimicking entire installed base in a fab

(*) Manufacturing Execution System

Verify Fast using functional models and realistic data

Ensuring a *correct* data flow with function owners, SW Integration and System Performance.



Test design and test methodology in collaboration with TNO-ESI

Legend

system interface (customer)

simulator interface (non-customer)

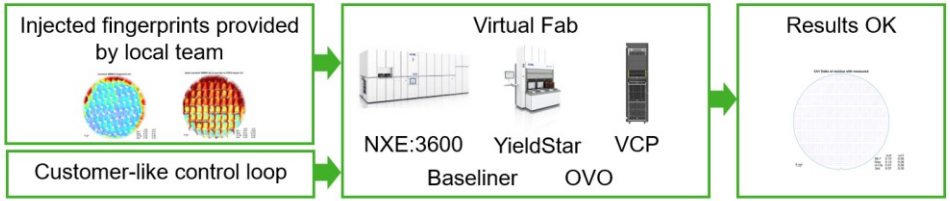
ASML

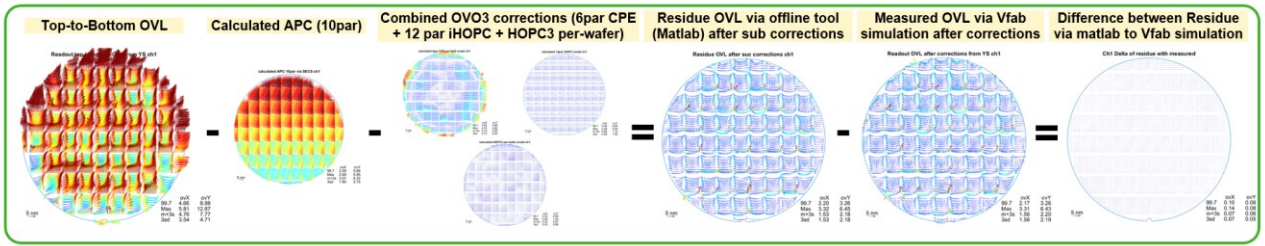
Verify Fast → Holistic Digital Twin results

The ‘Turing test’ of Lithography

Successfully tested real-life use-case without the real-life HW and costs

Verified combined NXE:3600/OVO/Baseliner/VCP/YS using customer machine data and injected fingerprints





APC = Automatic Process Correction
CPE = Corrections Per Exposure
HOPC = High Order Process Correction
IHOPC = Intrafield High Order Process Correction
OVO = Overlay Optimizer
OVL = Overlay
VCP = Virtual Computing Platform

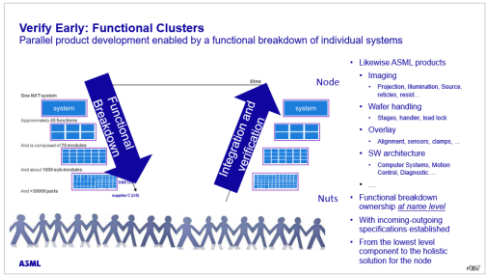
Functional performance testing using realistic customer data, workflow and products configurations

Adding functional models describing system behavior the Holistic Digital Twin can be used for product development

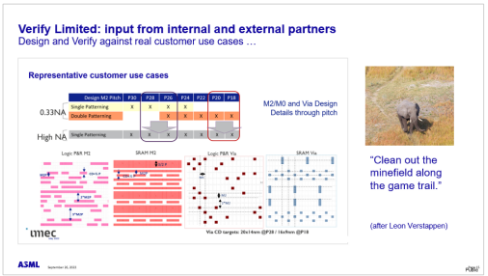
	OVL X (nm)	OVL Y (nm)
99.7%	0.10	0.06
Max	0.14	0.08

From Nuts to Nodes along the game trail

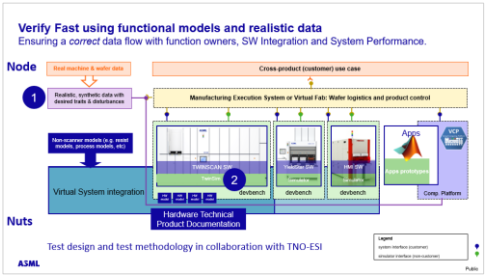
Integrating and verifying the complexity and diversity of lithographic manufacturing



Verify Early



Verify Limited



Verify Fast

With special thanks:

Rick Smetsers, Svetla Matlova, Timon Fliervoet, Paul van Gorp, Niels Braspenning, Ruud Teunissen, John Koster