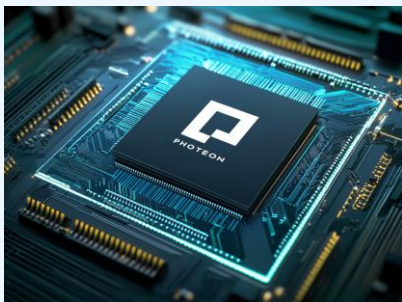


# Microcontroller #PSRV series

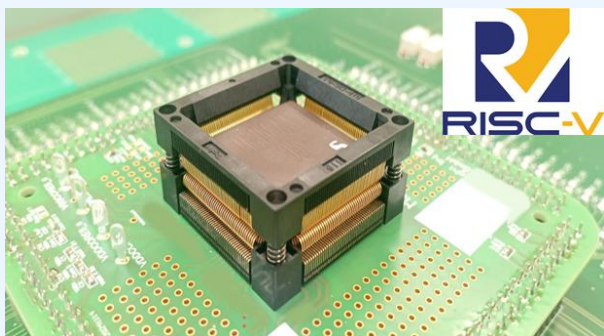


## APPLICATIONS



- Automotive
- Industrial
- Data Center
- Telecom
- Consumer
- Medical
- General Purpose

## OPEN-SOURCED



## ORDER INFORMATION

### Product Link

tbd

### Product Summary

Order Code	PSRVxxxx
Package	LQFP, QFP, WLCSP
Packaging	Tape & Reel, Tray

## PRODUCT FEATURES

- RISC-V Based Architecture
- Functional Safety, ASIL-D
- Multi-Zone Scalability: Application, Communication, DSP
- Adaptable & Unconstrained Memory
- 64-bit Capable at 1GHz
- Fast ADC: Software & Digital Control Loop
- AI Ready: Vector Oriented Matrix
- Time Resolution
- Domain Driver
- IP: Bus, Memory, Analog, Safety, Comms, Control
- Efficient Power Management
- Embedded Sensor Capability
- Software Development Support
- Your-IP: Protect It

**Control your Controller**



**Full Flexibility**  
Unconstrained Memory  
Configurable processing Zones



**1-N Cores**  
Only the Cores You Need



**Super Scalable ADC**  
Nx 16-Channel ADC



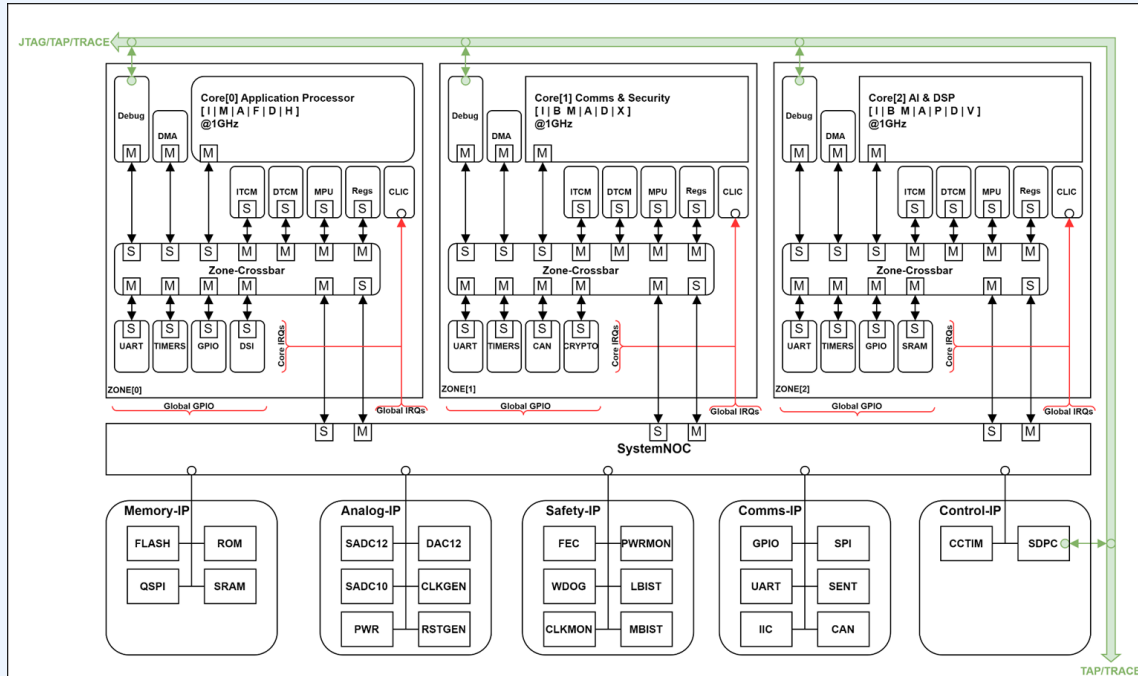
**AI Ready**  
Vector and Matrix processing  
Unit

# Microcontroller

## #PSMCxxxx



### SCALABLE SYSTEM



There may be one or many Processing-Zones, how many depends on the Customer-Application's Functional, Security & Safety Requirements. Reference design shows 3 such Processing-Zones, each tailored for specific needs.

### Common Peripherals

#### Bus-IP:

- High bandwidth NOC, non-blocking access
- Point to Point NOC integrity checks

#### Memory-IP:

- Embedded Flash, 8MB of Non-volatile memory
- ROM, Root of trust, boot-code
- QSPI, Quad SPI with XIP
- SRAM, 64 of general-purpose SRAM

#### Analog-IP:

- 2x 12bit SADC with 32 Channels at 1MS
- 1x 10bit Fast ADC at 10Mz
- 1x 10bit Fast ADC at 10Mz
- 12bit DAC at 1MS
- PWR, power management, trimming
- CLKCTL, Clock generation and Control, XTAL, PLL, IRC, Dividers

#### Safety-IP:

- Fault Event Collector
- Watchdog Timer
- Clock Monitoring
- Power Monitoring
- MBIST
- LBIST

#### Comms-IP:

- GPIO
- UART
- IIC
- SPI
- SENT
- CAN

#### Control-IP:

- Complex Control Timers
- Software Defined Power Controller

#### Your-IP:

- You have it, we can integrate it

# Microcontroller

## #PSMCxxxx



### PRODUCT FEATURES

#### Processing Zones

**Zone[0]:** Application processor with optional Hyper-Visor extension to host an OS

- CPU: RISC-V [ I | M | A | F | D | H ] running at 1GHz
- Instruction & Data Tightly Coupled Memories, 8KB and 8KB respectively.
- MPU, Memory Protection Unit
- CLIC, pre-emptive, low-latency, vectored, priority/level-based handling.
- DMA, Direct Memory Access
- Private Peripherals:
  - UART, Universal Asynchronous Receiver and Transmitter, for debug and status
  - SYSTIM, System timer for scheduling and measurement
  - GPIO, General Purpose IOs for Input and Output
  - DSI, Display Serial Interface for off chip display connectivity

**Zone[1]:** Communication and Security for handling secure transfer of data into and out of the device

- CPU: RISC-V [ I | B | M | A | D | X ] running at 1GHz
- Instruction & Data Tightly Coupled Memories, 8KB and 8KB respectively.
- MPU, Memory Protection Unit
- CLIC, pre-emptive, low-latency, vectored, priority/level-based handling.
- DMA, Direct Memory Access
- Private Peripherals:
  - UART, Universal Asynchronous Receiver and Transmitter, for debug and status
  - SYSTIM, System timer for scheduling and measurement
  - CAN, Controller Area Network
  - CRYPTO, Cryptography Accelerators: AES, HASH, Secure-Boot, Secure-Communication, PKE.

**Zone[2]:** AI & DSP to handle bulk data processing using SIMD instructions and matrix operations

- CPU: RISC-V [ I | B | M | A | P | D | V ] running at 1GHz
- Instruction & Data Tightly Coupled Memories, 8KB and 8KB respectively
- MPU, Memory Protection Unit
- CLIC, pre-emptive, low-latency, vectored, priority/level-based handling
- DMA, Direct Memory Access
- Private Peripherals:
  - UART, Universal Asynchronous Receiver and Transmitter, for debug and status
  - SYSTIM, System timer for scheduling and measurement
  - GPIO, General Purpose IOs for Input and Output
  - SRAM, Data RAM for input/output data from SADC12 samples for processing