FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

Accessing the FAMES Pilot Line

Susana Bonnetier

Open-Access Chairperson - CEA-Leti

Chips JU

Outline

1. What do we mean by Open-Access?
2. What are the Open-Access mechanisms?
   - Gaining access to the FAMES technologies
3. What technologies are or will be available in 2026?
   - Consulting the FAMES Open-Access webpage
   - Submitting a User Request
4. Upcoming FAMES events – let's meet again!

What do we mean by Open-Access ?

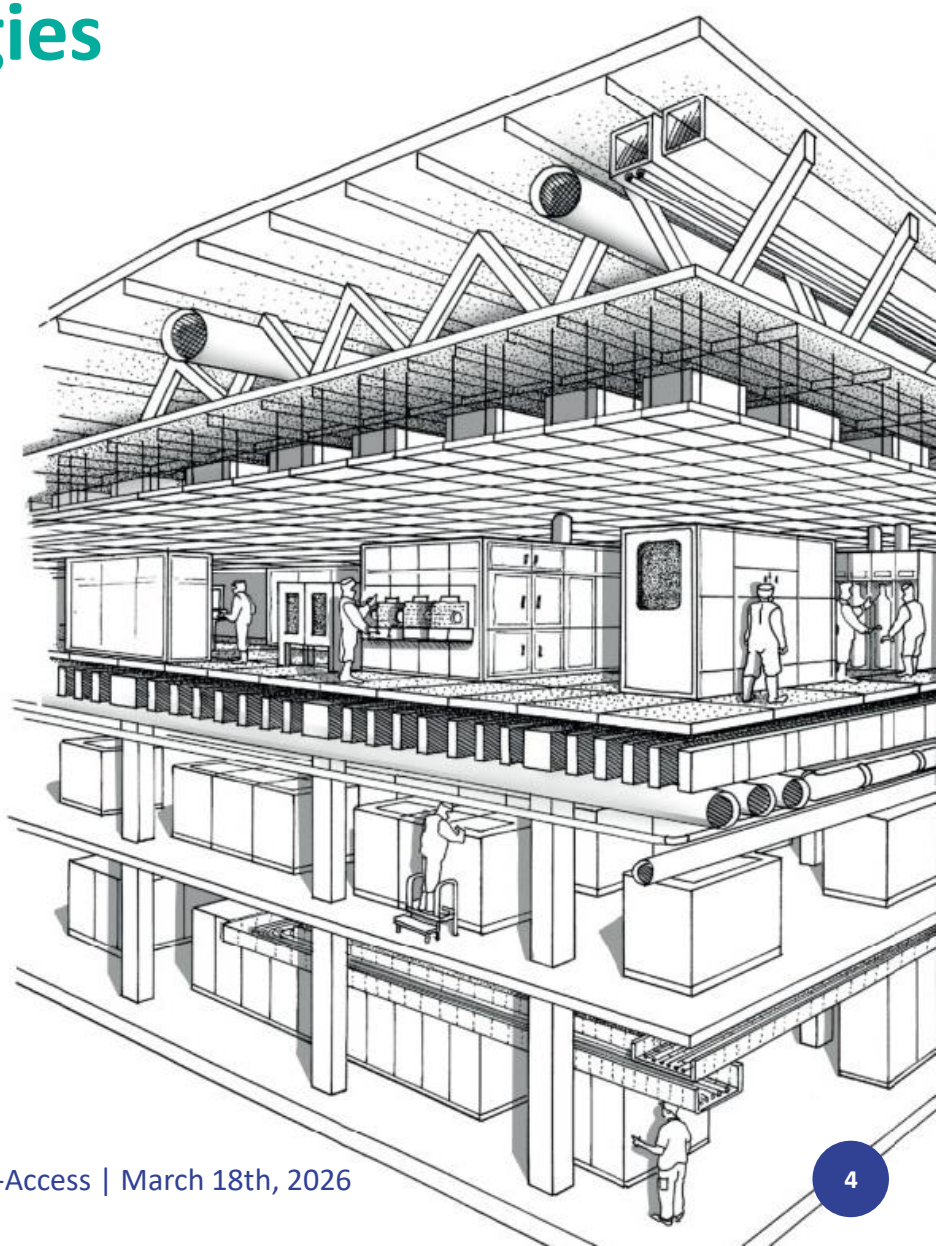
FAMES European Open-Access Pilot Line for Advanced Semiconductor Technologies

To facilitate the adoption of the sovereign FAMES Technologies

To gain access to:

- Two types of PDKs (multi-project wafer or IC design assessment)
- FAMES technologies (FD-SOI advanced nodes, embedded non-volatile memories, RF components, 3D integration options) for performance evaluations
- Specific process steps, modules, integration flows, and demonstrator results

as they become available



The FAMES Pilot Line is open to all types of Users

LARGE COMPANIES

SMEs

START-UPs

RESEARCH COMMUNITY

Design Houses
Fabless
Foundries
Integrated Device Manufacturers
Material and Tool Suppliers
Universities
Research Centers

Leveraging the FAMES Pilot Line Technologies

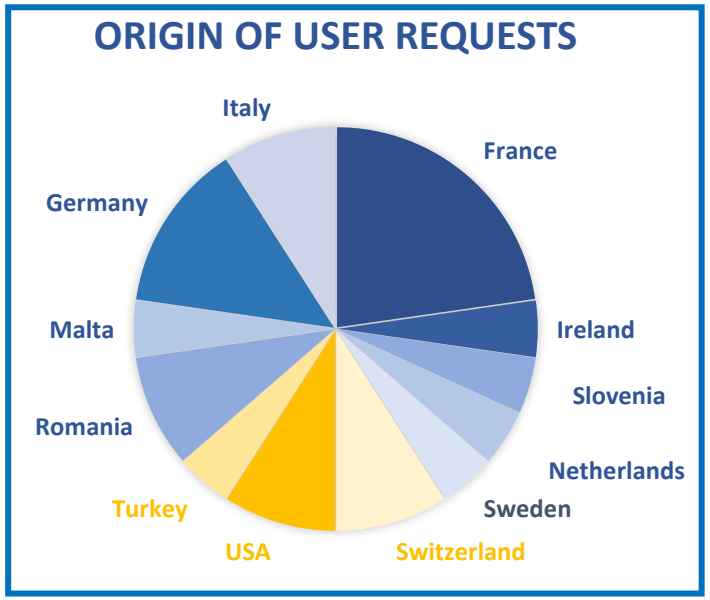
- Design innovative integrated circuits using the FAMES Pathfinding PDKs
- Test the unique capabilities of specific circuit designs through MPW opportunities
- Develop customized R&D solutions using novel technological modules to address your specific needs
- Count on FAMES up-to-date tools and processes to fabricate new technological features
- Generate new IP through advanced developments thanks to the FAMES Pilot Line
- Imagine new solutions for specific markets inspired by FAMES demonstrators

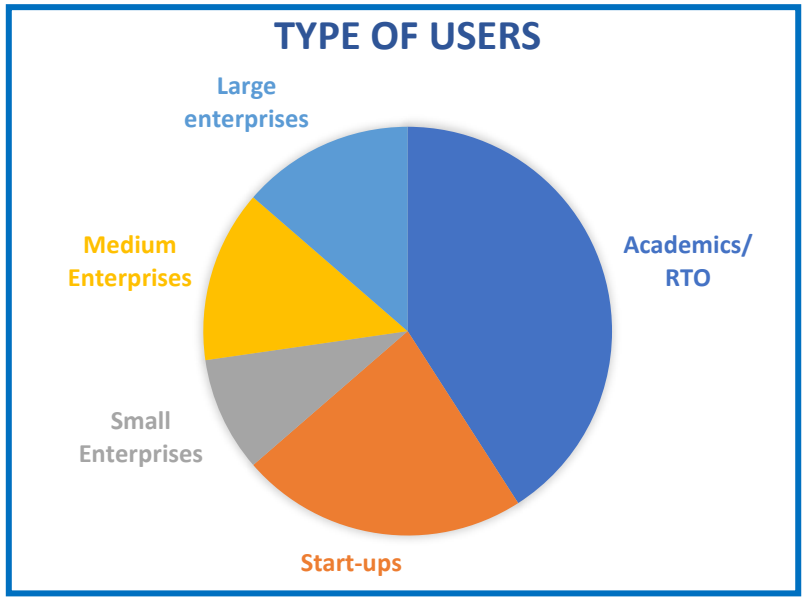
MPW: Multi-Project Wafers allow customers to share tooling (such as masks) and microelectronics wafer fabrication costs by mutualizing several designs or projects

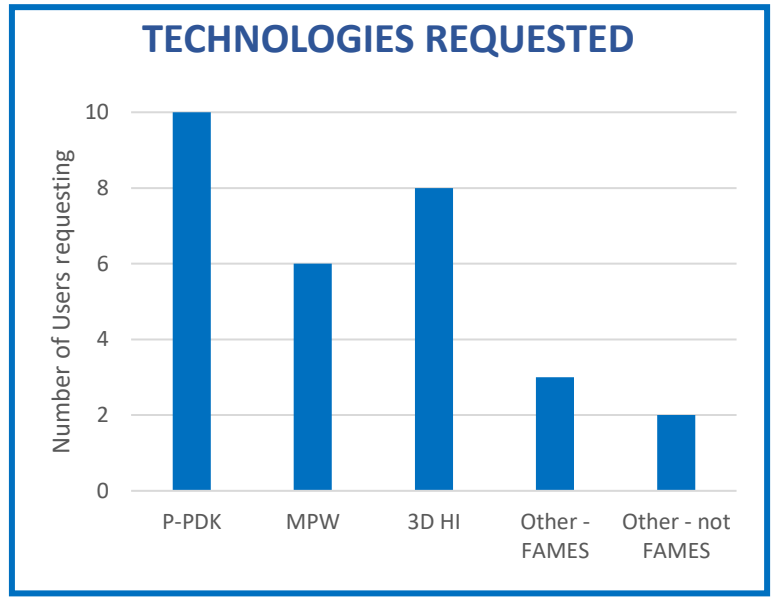
2025 User Requests

A total of 22 requests from multiple domains:

Telecommunications, Cognitive and Edge AI, Power Management, Memories, Smart Substrates...







What are the Open-Access Mechanisms?

Two ways for Users to access the FAMES Pilot Line

Yearly Open-Access Calls
March to May

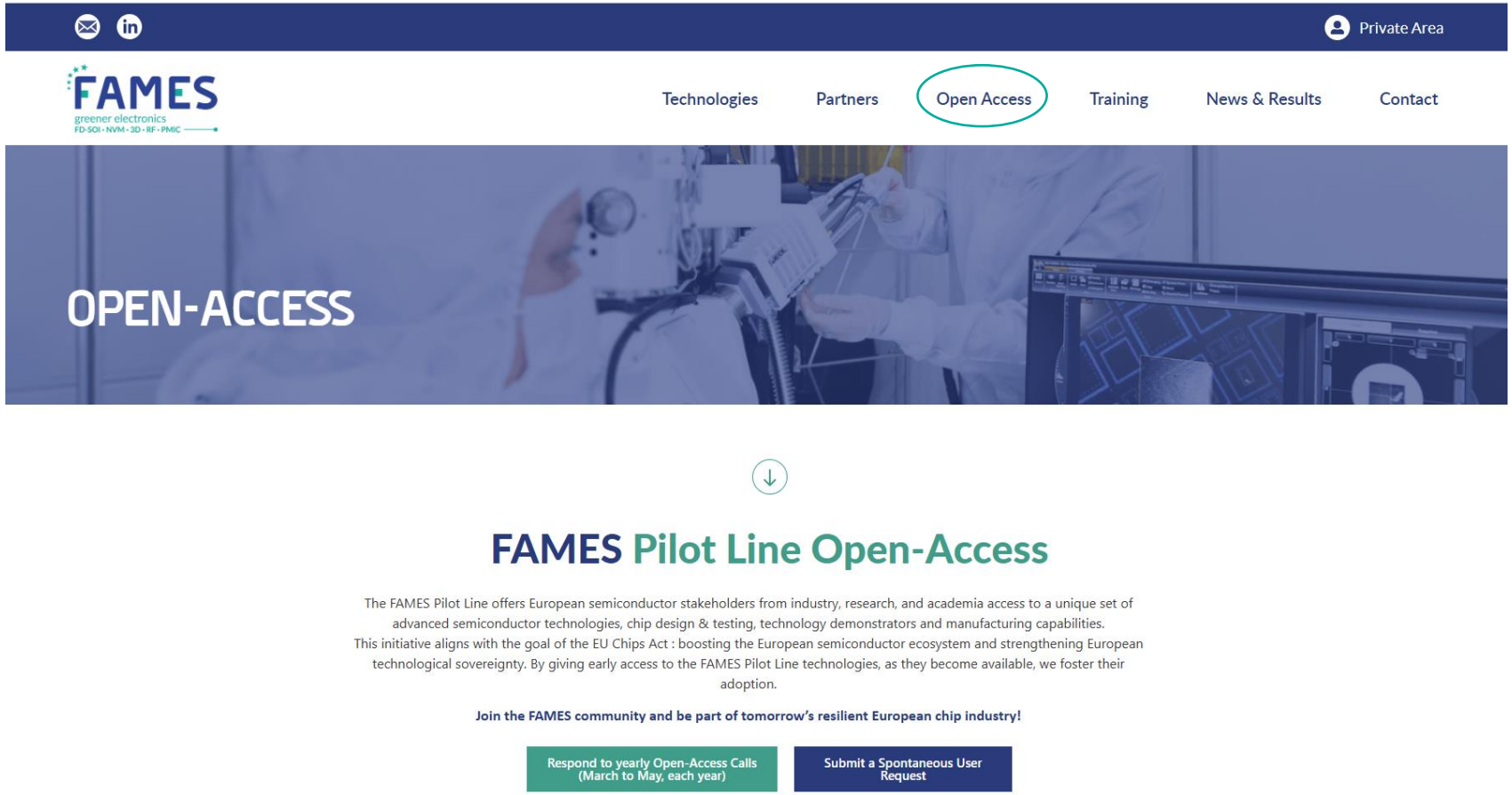
fames-pilot-line.eu

Spontaneous Requests
All year round

fames-pilot-line.eu

Chips JU Competence centers and EuroCDP Design Platform

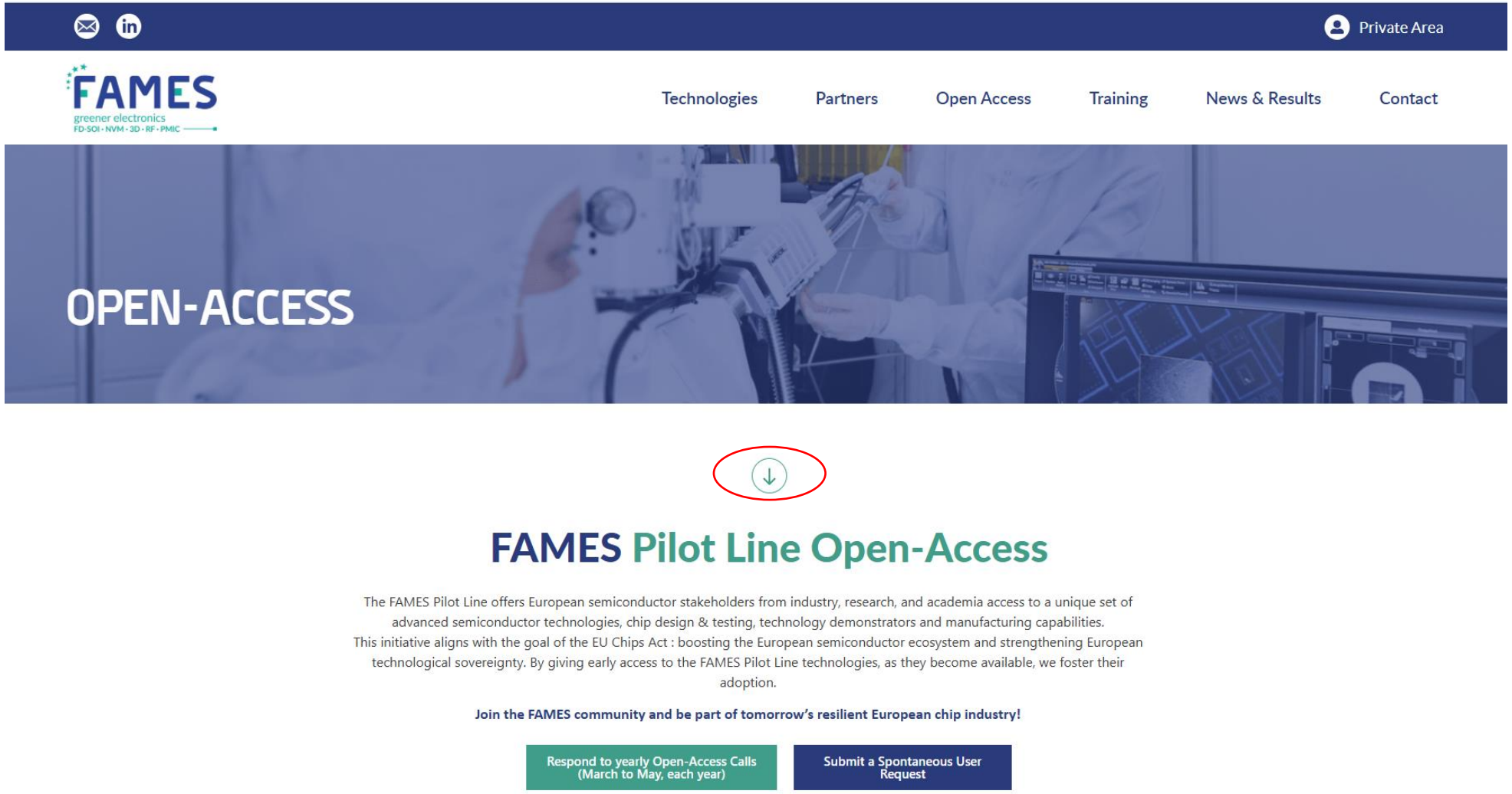
Website: New 2026 Open-Access page



https://fames-pilot-line.eu/open-access/

FAMES Technologies Available in 2026

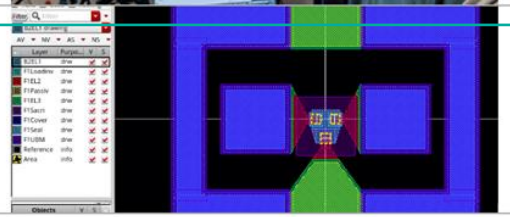
Website: New 2026 Open-Access page



2026 Open-Access Technology Portfolio

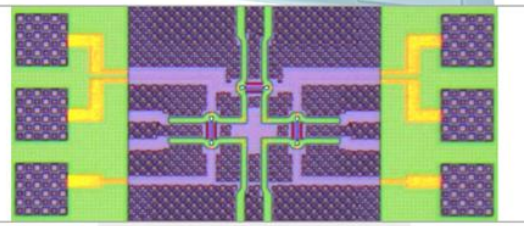
FD-SOI 10nm Pathfinding PDK +

15 GHz LiNbO3 BAW filters +

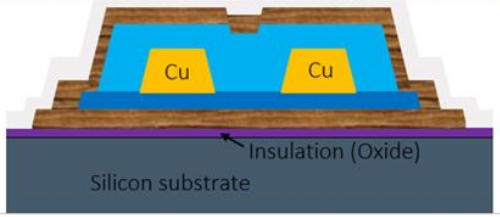


7-15 GHz AlN/ScAlN RF filters +

PCM RF switch demonstrators +



PMIC options: Magnetics on Silicon +



FD-SOI 10nm Pathfinding PDK - 1st release

FD-SOI 10nm Pathfinding PDK –

Overview

FAMES is currently offering a Pathfinding PDK to evaluate the performance of the 10nm FD-SOI CMOS technology. Based on process and device TCAD simulations and silicon data, this first release allows for assessment of digital circuits. Process assumptions are based on the most recent generations of FD-SOI technology enabling 68nm CPP and 48nm metal pitches. It contains 16 logic standard cell libraries (see below for more detail) with several threshold voltage flavors (multi-V_{th}), 2 poly-bias options, SPICE models, tools for physical verification and a parasitic extraction tool for post-layout simulations.

Based on virtual advanced FD-SOI technologies, this PDK will allow users to create new design architectures that benefit from Body bias compensation, mechanical stress engineering for both NMOS and PMOS devices, and new routing solutions, among others.

Expected timeline

Release 1, for digital circuits, is available.

Release 2, which will have analog and RF options too, will be available Q1 2027.

Access and technical support

Users may obtain access to FAMES Pathfinding PDKs by signing an NDA and a Design Kit License Agreement. A collaborative approach will be preferred.

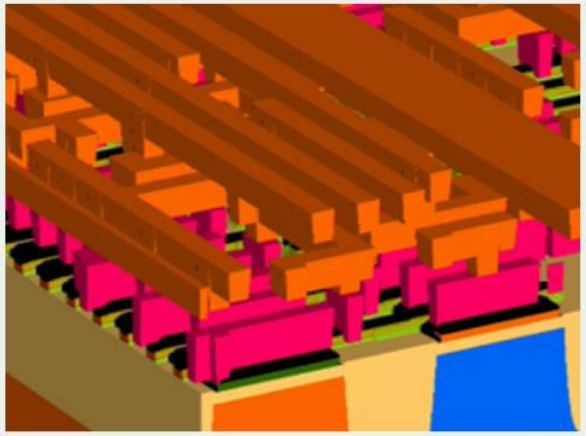
FAMES Pathfinding PDK users will have access to technical support from FAMES experts and the possibility of building and publishing model case studies with one or more FAMES partners.

PDK Specifications and Contents

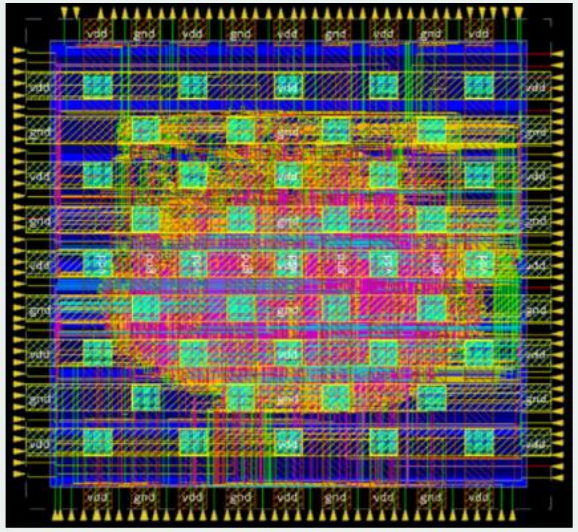
- Design Rule Manual
- Device library including multi-V_{th} MOSFET for schematics and layouts
  - 4 V_{th} flavors (SLVT, LVT, RVT, HVT)
  - 2 poly-bias options for digital devices + CPP 136nm analog option
  - SRAM transistors: pass gate, pull-up and pull-down
- Device model library supporting multi-V_{th} solutions for SPICE simulation
- Process variability and corner support
- DRC/LVC deck files for physical verifications
- PEX extraction tool

Enabling tools required

- Design/Layout: Virtuoso® Layout Suite (Cadence)
- Electrical Simulation: Xpedition AMS (Siemens EDA),HSPICE® (Synopsys) and Spectre (Cader
- Physical Verification (DRC/LVS): Calibre® (Siemens EDA)
- Parasitic Extraction (PEX): StarRC® (Synopsys)
- Place and Route: Innovus® (Cadence)



Credit: CEA-Leti – SEMulator3D®



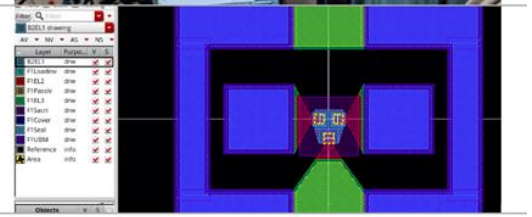
Credit: CEA-Leti – FIR filter circuit top view

Respond to the Open-Access Call

2026 Open-Access Technology Portfolio

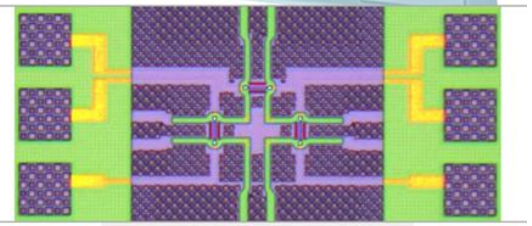
FD-SOI 10nm Pathfinding PDK +

15 GHz LiNbO3 BAW filters +

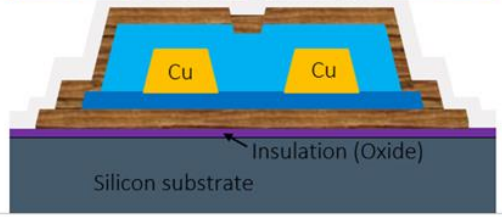


7-15 GHz AlN/ScAlN RF filters +

PCM RF switch demonstrators +



PMIC options: Magnetics on Silicon +



15 GHz $LiNbO_3$ RF Bulk Acoustic Wave (BAW) Filters

15 GHz LiNbO3 BAW filters –

Overview

FAMES offers a 200 mm platform dedicated to a Solidly Mounted BAW Resonator filter technology platform. This offers an opportunity to design and fabricate custom prototype filters that can be integrated on foundry interposers and/or RF-ICs.

FAMES is developing innovative acoustic filter technologies to address the FR3 frequency range (7-24 GHz). This is made possible by the integration of high-coupling piezoelectric materials such as lithium niobate.

This innovative BAW-SMR technology will provide highly miniaturized band pass filtering capabilities to RF systems in the FR3 range, and could advantageously replace conventional microwave filters in wireless systems.

Expected timeline

A PDK dedicated to filters intended to operate near a centre frequency of 15 GHz will be available **Q2 2026**.

Design your specific BAW-SMR filter in time to meet the design freeze planned for end 2026.

Access and technical support

To access the FAMES BAW-SMR filter PDK, Users must sign an NDA and a Design Kit License Agreement (DKLA). The price of R&D samples will depend on the User's specific RF Filter Design.

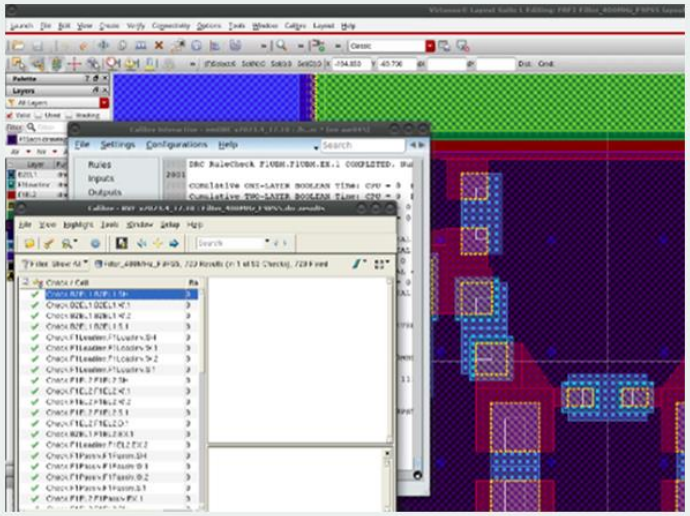
FAMES PDK users will have access to technical support from FAMES experts.

PDK Specifications and Contents

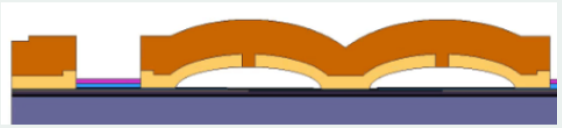
- Design Rule Manual – for this custom technology
- Device Library including parametric cells for layouts
- Device models for circuit and circuit/electromagnetic coupled simulations
- Process variability support
- DRC check for physical verifications

Technological features

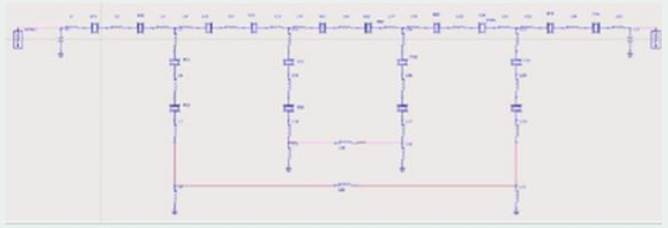
- 200 mm custom technology
- Add-on possible for wafer level thin film packaging (WLTFP) of the resonators/filters
- 5 mask levels (9 with WLTFP option)



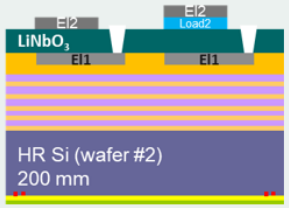
Layout environment illustration. Credit : CEA-Leti – Cadence Virtuoso®; Siemens EDA Calibre®



To scale model of a filter cross-section with its thin-film packaging. Credit: CEA-Leti



ADS simulation circuit illustration. Credit: CEA-Leti – Keysight ADS®



Schematic of a BAW filter stack @ 15GHz. Credit: CEA-Leti

Enabling tools required

- Analog circuit design: Advanced Design System® (Keysight)
- Layout: Virtuoso® (Cadence)
- Physical verification (DRC): Calibre® (Siemens EDA SW)

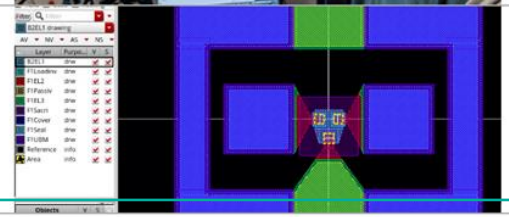
If you would like to obtain any of these additional services, please mention it on the User Request submission form in the comments area.

Respond to the Open-Access Call

2026 Open-Access Technology Portfolio

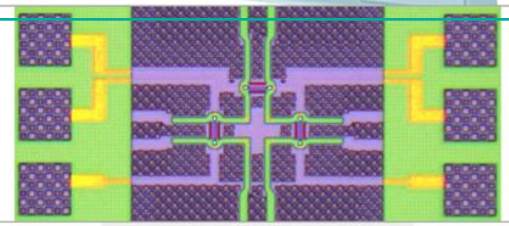
FD-SOI 10nm Pathfinding PDK +

15 GHz LiNbO3 BAW filters +

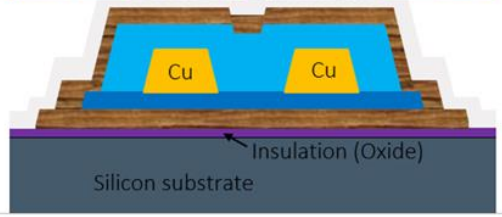


7-15 GHz AlN/ScAlN RF filters +

PCM RF switch demonstrators +



PMIC options: Magnetics on Silicon +



7-15 GHz AlN/ScAlN RF BAW Filters

7-15 GHz AlN/ScAlN RF filters –

BAW resonator R&D Services: RF AlN/ScAlN filter (7-15GHz)

Overview

FAMES offers a 200 mm platform of FBAR filters targeting the 7-15 GHz range (lower frequencies are also possible). The platform is based on highly piezoelectric ScAlN films and low resistance multilayer electrodes optimized for high frequencies. This is a pre-release ("beta") offer allowing Users to evaluate the platform's potential.

Expected timeline

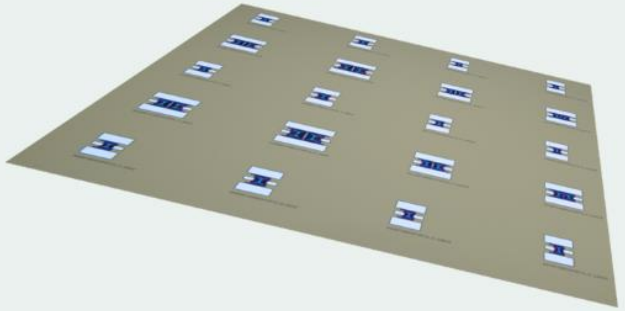
The PDK for the AlN/ScAlN RF Filter platform is expected Q4/2026.

Users must sign an NDA and a Design Kit License Agreement (DKLA) before gaining access to the PDK. A collaborative approach will be preferred. PDK Users will have access to technical support from FAMES experts.

Description of Services

Evaluation of FR3 ScAlN BAW resonator and filter processes

- RF filter test samples
  - Can be manufactured in the 7-15 GHz range.
  - Frequencies below 7 GHz also possible, within certain process variations.
- Test resonator designs
  - Test resonators can be manufactured to User specified frequencies.
  - For plain resonators, some layouts are available.
- RF filter design support
- Limited device and process design rule guidance available.
- Wafer level characterization (S-parameters) available.



High frequency BAW resonator test structures. VTT Technical Research Centre of Finland.

RF Filter Platform

- $Sc_xAl_{1-x}N$ (x=0.2, 0.3) films.
- Low sheet resistance multilayer electrodes.
- Restrictions in film thicknesses/frequency ranges. Assessment per customer request.
- Ion beam trimming for thickness & frequency accuracy presently limited to the end of the process; in-line trimming will be available in 2027.

Estimated price and fabrication time:

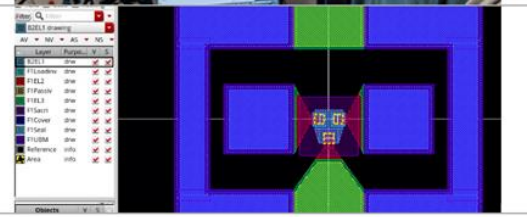
- RF resonator/filter test samples take 16-20 weeks to be produced.
- Characterisation time estimated at 4-6 weeks.
- Price will vary as a function of the test samples and services requested.
- Estimated delivery dates will take into account the process line load.

Respond to the Open-Access Call

2026 Open-Access Technology Portfolio

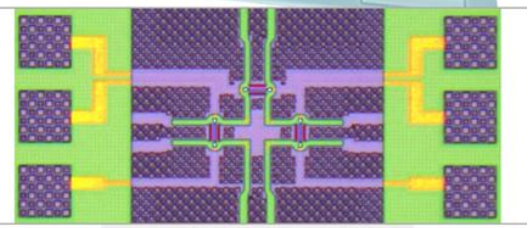
FD-SOI 10nm Pathfinding PDK +

15 GHz LiNbO3 BAW filters +

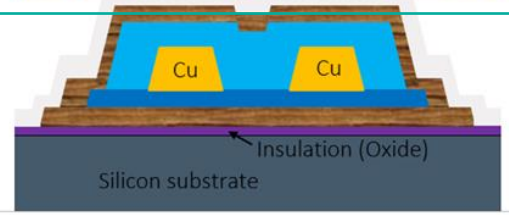


7-15 GHz AlN/ScAlN RF filters +

PCM RF switch demonstrators +



PMIC options: Magnetics on Silicon +



PCM RF Switch Demonstrators

PCM RF switch demonstrators –

PDK to access an RF Switch demonstrator based on a Phase Change Material

Overview

FAMES is integrating, onto a 300 mm technology platform, RF Switches based on PCM (Phase-change chalcogenide materials), having a Figure of Merit (FOM = RON*COFF) < 10 fs. This technology can be positioned within a CMOS Back-End-of-Line (BEOL) to enrich the technological offer of semiconductor foundries.

A PDK (Release1) will give access to silicon by way of an MPW, allowing Users to design specific PCM RF switch demonstrators.

Expected timeline

The FAMES PCM RF switch technology will be accessible in 2026. A first release of the PDK is expected by Q4 2026 and will allow Users to implement specific designs on a high resistive silicon substrate. Users interested in this technology should submit a Spontaneous Request post Q2 2026.

Access and technical support

To access the FAMES PDK for PCM RF switch Users must sign an NDA and a Design Kit License Agreement (DKLA). The price of R&D samples will depend on the User's specific RF Switch design.

FAMES PDK Users will have access to technical support from FAMES experts

Enabling tools required

- Layout: Virtuoso® Layout Suite (Cadence)
- Physical verification (DRC): Calibre® (Siemens EDA SW)

PDK Specifications and Contents

- Design Rule Manual
- Device library including PCM core cell for schematics and layouts
- Device model for simulation
- DRC for physical verification

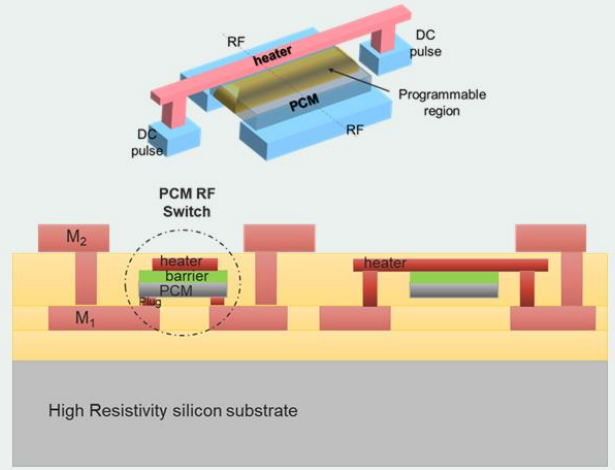
Technological features

- 300 mm High Resistivity Silicon Technology substrate
- 2 Metal layers + 1 resistive Metal layer (heater) + PCM layer

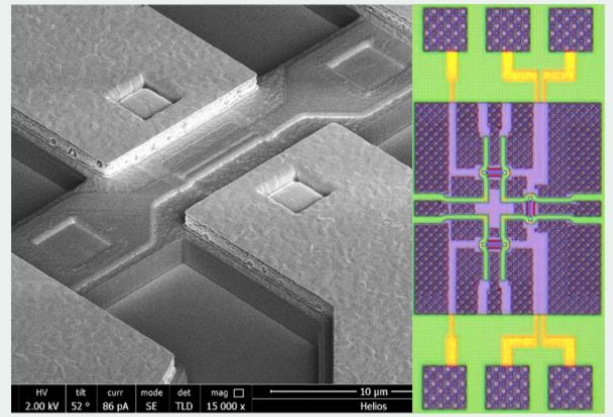
Other related R&D Services

- Design and layout expertise
- Circuit testing
- Expertise to analyse test results

If you would like to obtain any of these additional services, please mention it on the User comments area.



Schematic of a PCM RF Switch Release 1. Credit: CEA-Leti



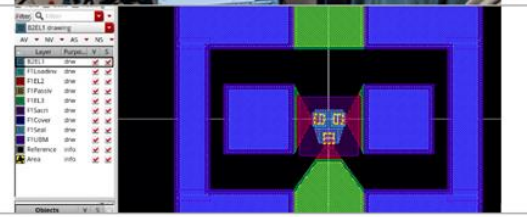
Optical microscope image of a Single- Pole Triple-Throw device based on PCM RF switch technology. Credit: CEA-Leti

Respond to the Open-Access Call

2026 Open-Access Technology Portfolio

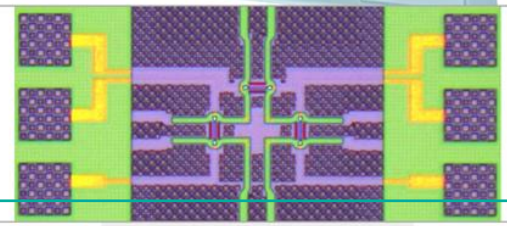
FD-SOI 10nm Pathfinding PDK +

15 GHz LiNbO3 BAW filters +

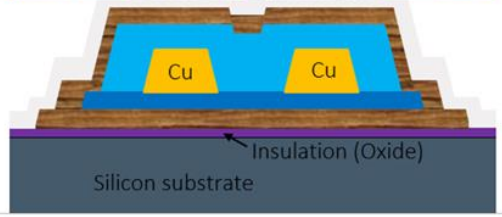


7-15 GHz AlN/ScAlN RF filters +

PCM RF switch demonstrators +



PMIC options: Magnetics on Silicon +



PMIC Options: Magnetics on Silicon

PMIC options: Magnetics on Silicon –

Overview

Powering integrated circuits using traditional Point of Load DC-DC converters is becoming a major concern because of the significant losses and parasitics that occur in the interconnect for the Power Delivery Network (PDN). This has led to a transition to granular arrays of integrated voltage regulators that deliver vertical power to ICs with minimal PDN losses and parasitics. A key enabler of this transition to Integrated Power has been the move from bulky inductors to miniaturized magnetics on silicon enabled by the use of power converters operating at frequencies in the range 10 to 100 MHz.

Within the FAMES Pilot Line, Tyndall National Institute is developing its integrated magnetics on silicon technology for application with customized Power Management Integrated Circuits (PMIC) and high-density trench capacitors. The technology, known as MagIC (making magnetics disappear onto silicon), can deliver a stripline micro-inductor (see Fig. 1a-b) and micro-transformer (shown as a coupled inductor in Fig. 1c-d) with a footprint of less than 2550 µm × 800 µm and a substrate thickness of 100 to 525 µm.

Inductances of 3 to 5 nH can be provided with Q > 8 for operation in the 10 to 50 MHz frequency range.

Expected timeline

Samples of these micro-inductors and micro-transformers will be accessible at the end of 2026/start of 2027. Interested Users should respond to this 2026 FAMES Open-Access Call.

Access and technical support

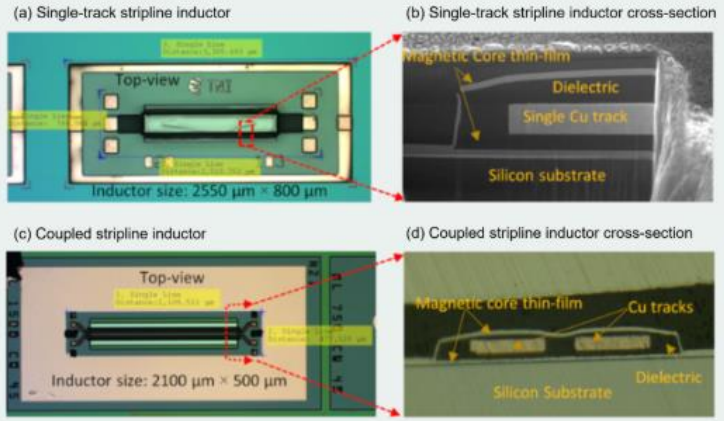
To receive samples of the FAMES Magnetics-on-Silicon, Users will be required to sign an NDA.

Users who gain access to FAMES's Magnetics-on-Silicon will have access to technical support from Tyndall experts.

Other related R&D Services

- DC-DC converter assembly, including inductors with User PMICs and capacitors
- Converter Circuit testing

If you would like to obtain any of these additional services, please mention it on the User Request submission form in the comments area.



(a) Top view of a Tyndall-fabricated Single-track stripline micro-inductor on silicon substrate, (b) Cross-section of a part of the single-track micro-inductor showing a single Cu track surrounded by the thin-film magnetic core, (c) Top view of a Tyndall-fabricated coupled stripline micro-inductor on silicon substrate, and (d) Cross-section of the coupled micro-inductor showing two Cu tracks surrounded by a thin-film magnetic core.

Inductor Specifications

- Inductor Parameters:
  - Single Strip-line Inductor: Inductance = 3 – 5 nH; Q > 8; Operating Frequency: 10 – 50 MHz
  - Coupled Strip-line Inductor: 3 – 5 nH; Coupling Coefficient = 0.5 – 0.7
- Inductor die thickness including substrate: max. 600 µm
- Substrate choices: Silicon and SOI
- Inductor footprint: max. 2550 µm × 800 µm (Including the bond pads and surrounding mechanical support area)
- Test Data and Deliverables for Samples Provided:
  - Measurement Data:
  - Inductance, DC Resistance (DCR), small-signal measured AC Quality Factor (Q) and saturation current (I_{sat})
  - Inductors bumped or copper plate exposure for flip-chip assembly
  - Device model for SPICE simulation
- Inductors bumped for with Flip-chip assembly

Respond to the Open-Access Call

Submitting a Request for the FAMES Technologies Available in 2026

Submission Form

FAMES Open-Access Call User Request

Please note that your answers will help us establish the eligibility of your request.

Name *
First name

Last name *
Last name

Email *
Email

Phone number
Phone number

Position *
Position within your organisation

Organisation *
Organisation name

Organisation website *
Organisation website

Organisation type *

DUNS number or SIRET number *
Organisation's DUNS or SIRET n

Organisation location *

City *
City

Street Address *
Street Address

Portfolio technologies you are requesting:

- [ ] FD-SOI 10nm Pathfinding PDK
- [ ] 15 GHz LiNbO3 BAW filters
- [ ] 7-15 GHz AlN/ScAlN RF filters
- [ ] PCM RF switch demonstrators
- [ ] PMIC: Magnetics on Si

Application(s) for which you are requesting this FAMES technology *

Aerospace
Automated systems
Automotive
Building materials

Comment/Explanation *
Please tell us more about your project and the application(s) you have in mind.

How did you hear about the FAMES Pilot-Line?

Prefered contact mode

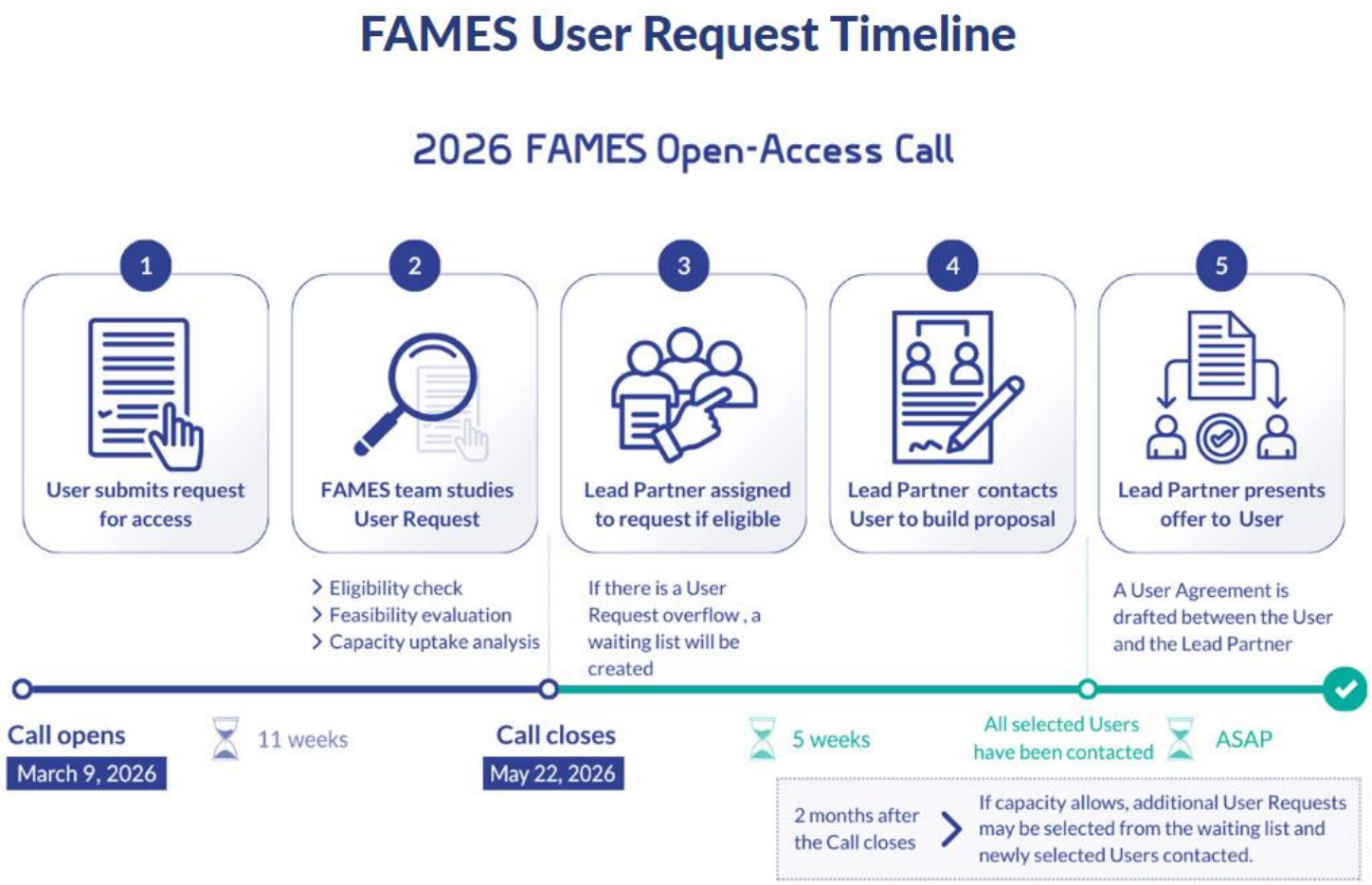
Acknowledgment *

- [ ] I have read and agree to the FAMES Privacy policy .

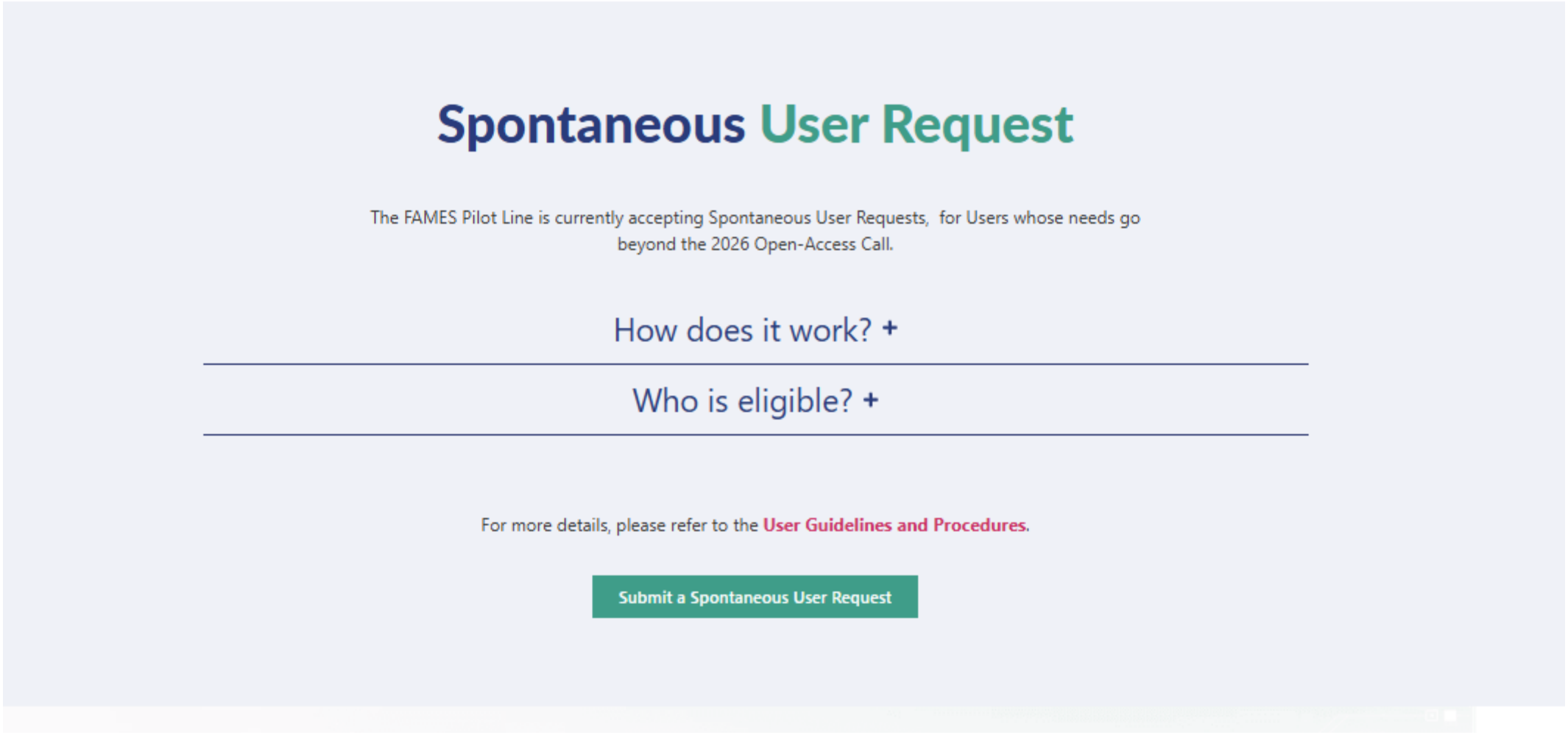
Submit

All FAMES Partners undertake to respect their obligations in application of regulations in force and, especially, regulation (EU) 2016/679 of the European Parliament and of the Council of 27 April 2016, on the protection of natural persons with regard to the processing of personal data and on the free movement of such data (referred to as "GDPR").

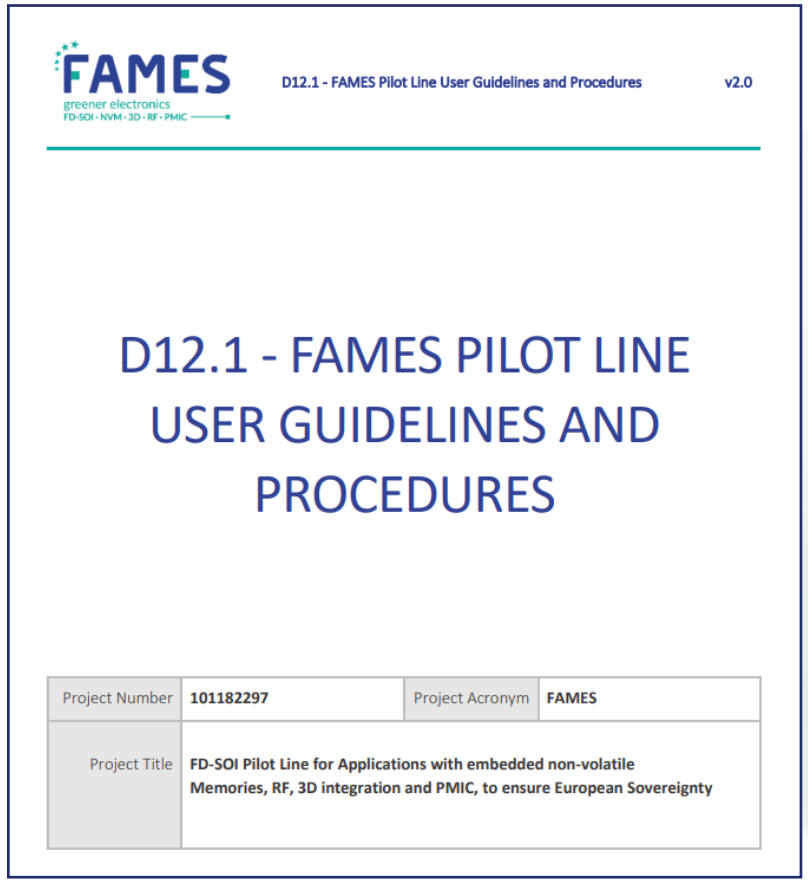
FAMES User Request Timeline



Two access modes



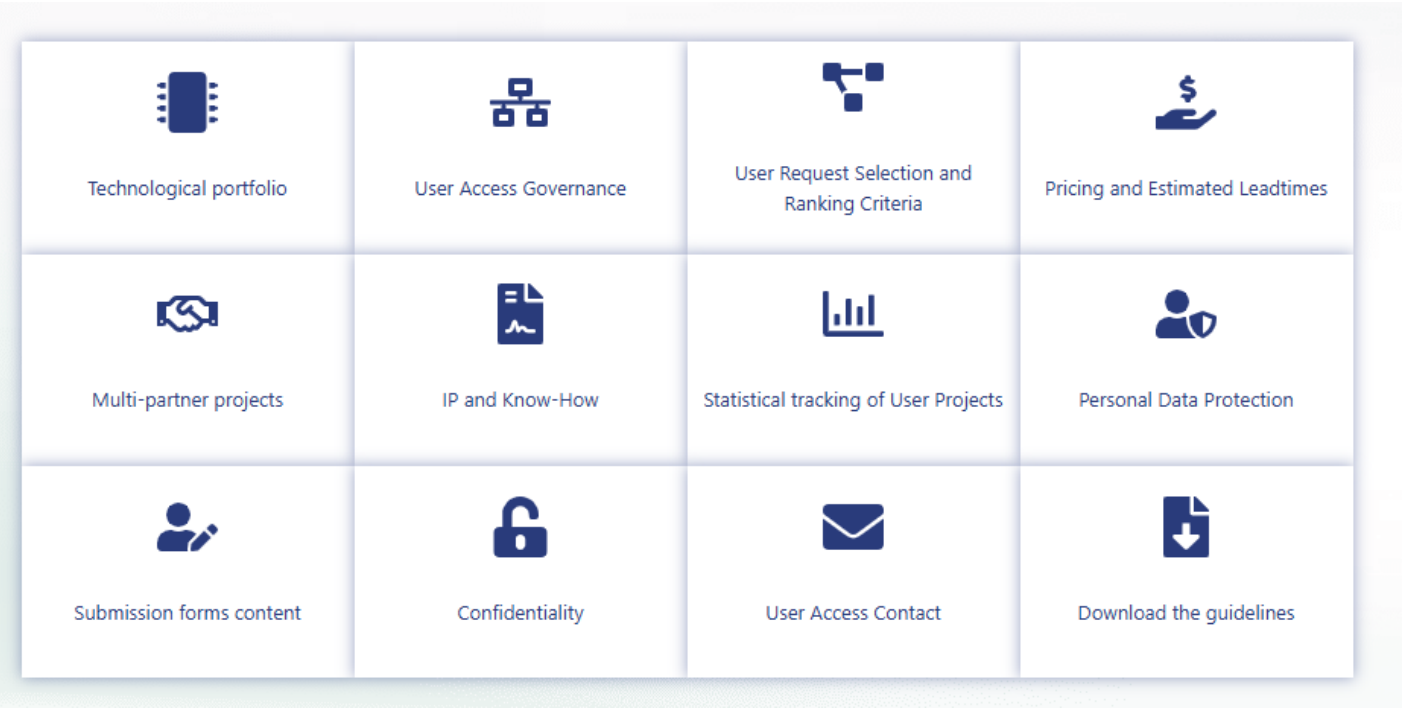
User Guidelines and Procedures


FAMES greener electronics FD-SOI · NVM · 3D · RF · PMIC

D12.1 - FAMES Pilot Line User Guidelines and Procedures v2.0

D12.1 - FAMES PILOT LINE USER GUIDELINES AND PROCEDURES

Project Number	101182297	Project Acronym	FAMES
Project Title	FD-SOI Pilot Line for Applications with embedded non-volatile Memories, RF, 3D integration and PMIC, to ensure European Sovereignty		



FAQs

Frequently Asked Questions

- How is a User Request's eligibility determined?
- When will I know if my request has been selected?
- If my User Request is not selected this year, when can I resubmit a request?
- When will the next FAMES Open-Access Call take place?
- What will be the cost of accessing the FAMES Pathfinding PDK?

  The PDK is accessible for free but requires signing an NDA and a Design Kit License Agreement (DKLA).

- How can I contact the FAMES Open-Access team if I have a question related to the submission form or the FAMES Open-Access technological offer?

Upcoming FAMES Events

UPCOMING EVENTS

March 23-24, 2026

Chips from the North

FAMES Technical Session

Helsinki, Finland

April 22, 2026

FAMES & ChipsWIN

Joint Event

Leuven, Belgium

May 20-22, 2026

EuroSOI-ULIS

FAMES Booth & talk

Granada, Spain

FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

Thank you

https://fames-pilot-line.eu/open-access/

FAMES

greener electronics

FD-SOI · NVM · 3D · RF · PMIC

cea leti

Tyndall National Institute
Institiúid Náisiúnta

SAL SILICON AUSTRIA LABS

VTT

imec

Fraunhofer MIKROELEKTRONIK

UCLouvain

Warsaw University of Technology
Centre for Advanced Materials and Technologies CEZAMAT

GRENOBLE INP UGA

UNIVERSIDAD DE GRANADA

SiNANO Institute

Chips JU

(2023 – 2028)

Sponsors

The FAMES Pilot Line of the Chips JU is funded by Horizon Europe and Digital Europe Programs and the National Public Authorities of the partners involved. Grants N° 101182279 and 101182297.

FAMES

greener electronics

FD-SOI · NVM · 3D · RF · PMIC

Follow us

@fames-pilot-line

Q&A

FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

Thank you

https://fames-pilot-line.eu/open-access/

Follow us
@fames-pilot-line