JIACO Instruments

Microwave Induced Plasma (MIP) for sample preparation in semiconductor failure analysis and reliability testing

December 9th, 2025

For: Fraunhofer

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JIACO Instruments; www.jiaco.com

- Founded in 2014 as a spin-off from Delft University of Technology based on PhD research
- 1st to market with atmospheric plasma decapsulation: patented plasma source and plasma etching process
- 30+ conference papers, journals & presentations solving industry challenges
- Global customer base with leading semiconductor companies
- Application development and machine manufacturing in the Netherlands
- Service support located in the Netherlands and S.E. Asia
- Product roadmap: applications, speed, form factor, software driven by user feedback
- >100 machines in the field @:

MIP | IC Decapsulation

- Automated atmospheric pressure MIP IC decapsulation
- Utilizing only Oxygen and patented Hydrogen-based recipes
- Artifact free decapsulation
- MIP is the global standard for tackling the semiconductor industry's most demanding decapsulation challenges

MIP+ | Die Level Etching

- The Next Generation in Semiconductor sample preparation. MIP+ extends MIP's proven capabilities from package-level to die-level etching.
- Selective recipes enabling localized delayering

MIP Decap 2.5D/3D Case: Underfill Removal – Bottom-up Localized Opening

Best poster paper

ISTFA/2024

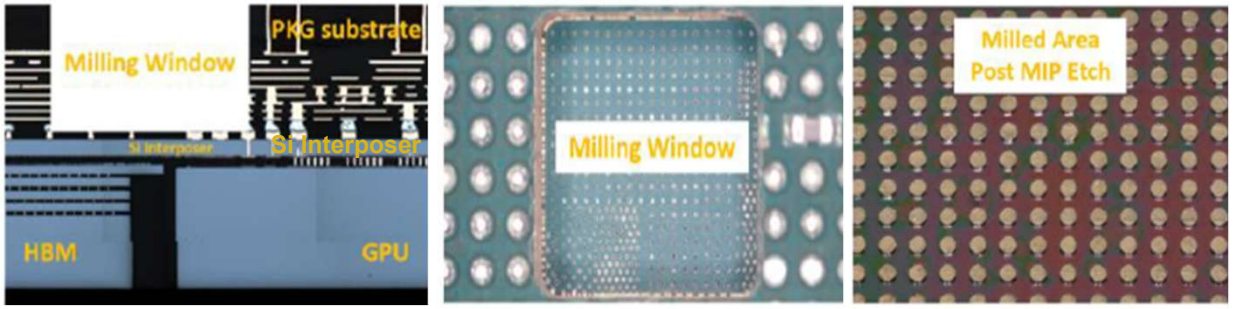
NVIDIA

Ref. Joseph Sanchez et al., ISTFA 2024

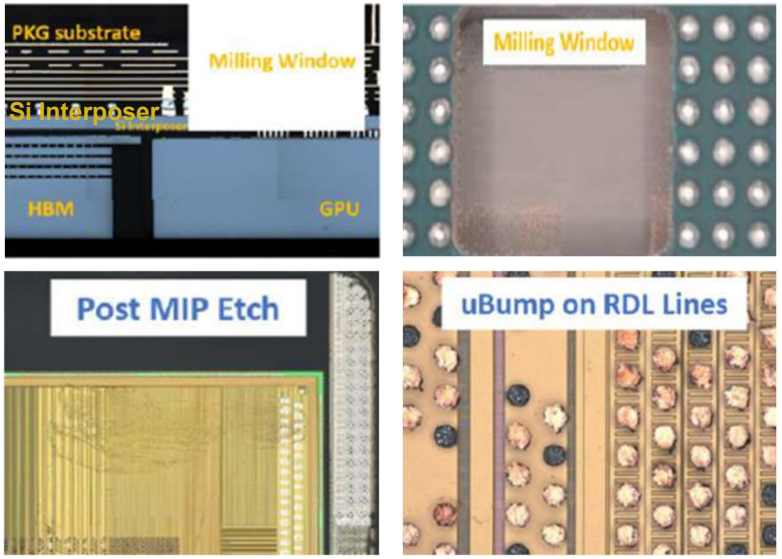
- **Challenge:** Precise and selective removal of underfill
- **MIP advantages**:
  - CF_4-free process (Ar + O_2 only) with high selectivity
  - Localized etching

Localized area µbump exposure process flow:

1. **Mechanical milling**
2. **MIP etch localized area to remove underfill**



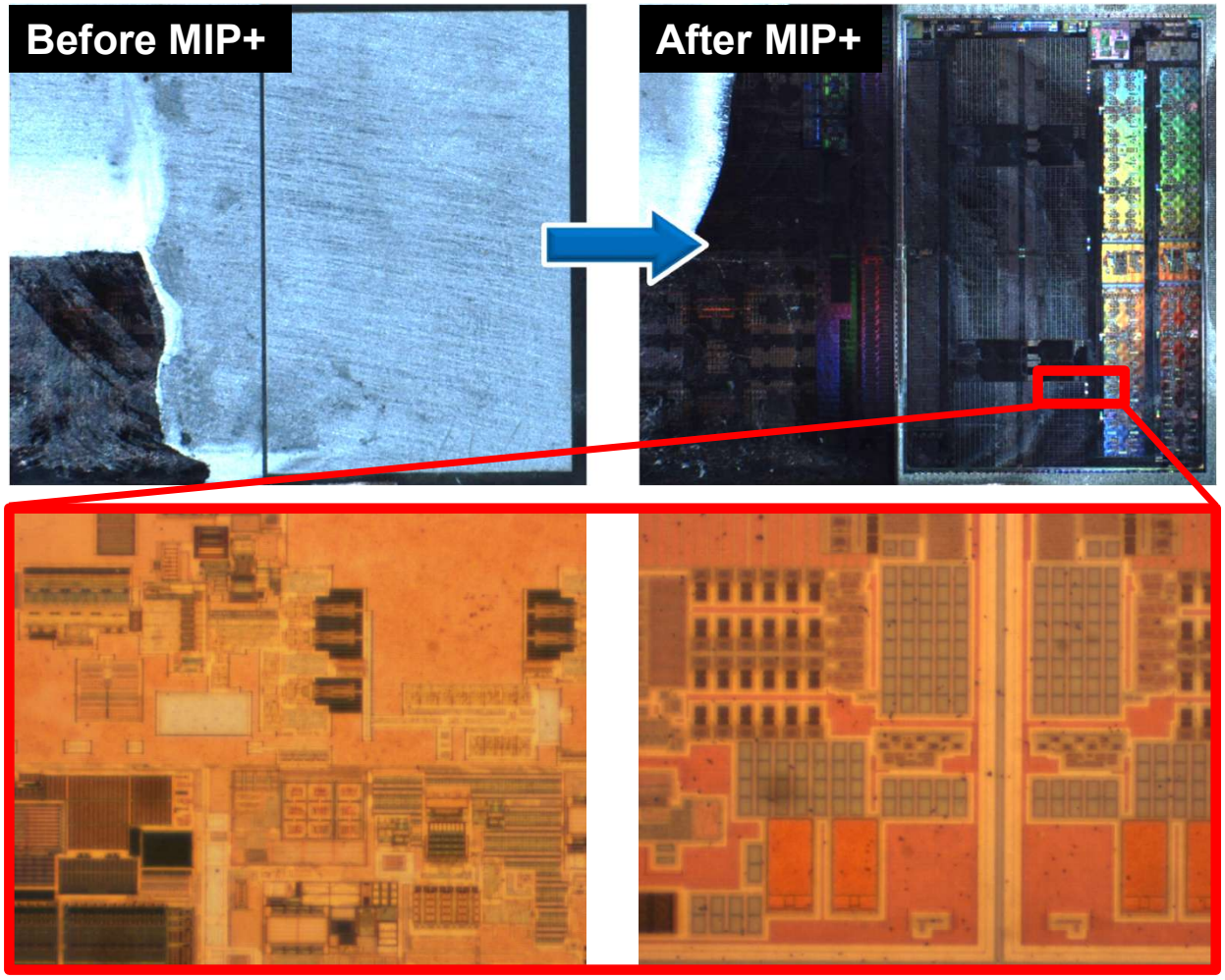
Case Study 1 focuses on the µbump interface between the package substrate and the silicon interposer.



Case Study 2 examines the µbump interface between the silicon interposer and the GPU die

MIP+ for die-level sample prep: Si die backside access
Bulk Si removal

ISTFA/2024



Localized removal of bulk Si to expose die circuitry from backside of the die

After processing, the die circuitry becomes visible

MIP Decap Case: System in Package (SiP)

- **Decap purpose:**
  - Localized die for FA
  - Faulty die or passive extraction
- **Difficulty of acid decapsulation:**
  Acid decap causes severe corrosion in the SiP module
- **MIP advantages**:
  Oxygen-based MIP can expose all the different components without inducing damage because of the extremely high selectivity.