CHIPNL Competence Centre

ChipNL Competence Centre Launch | 29 October 2025

Strengthening Design, Packaging & Equipment

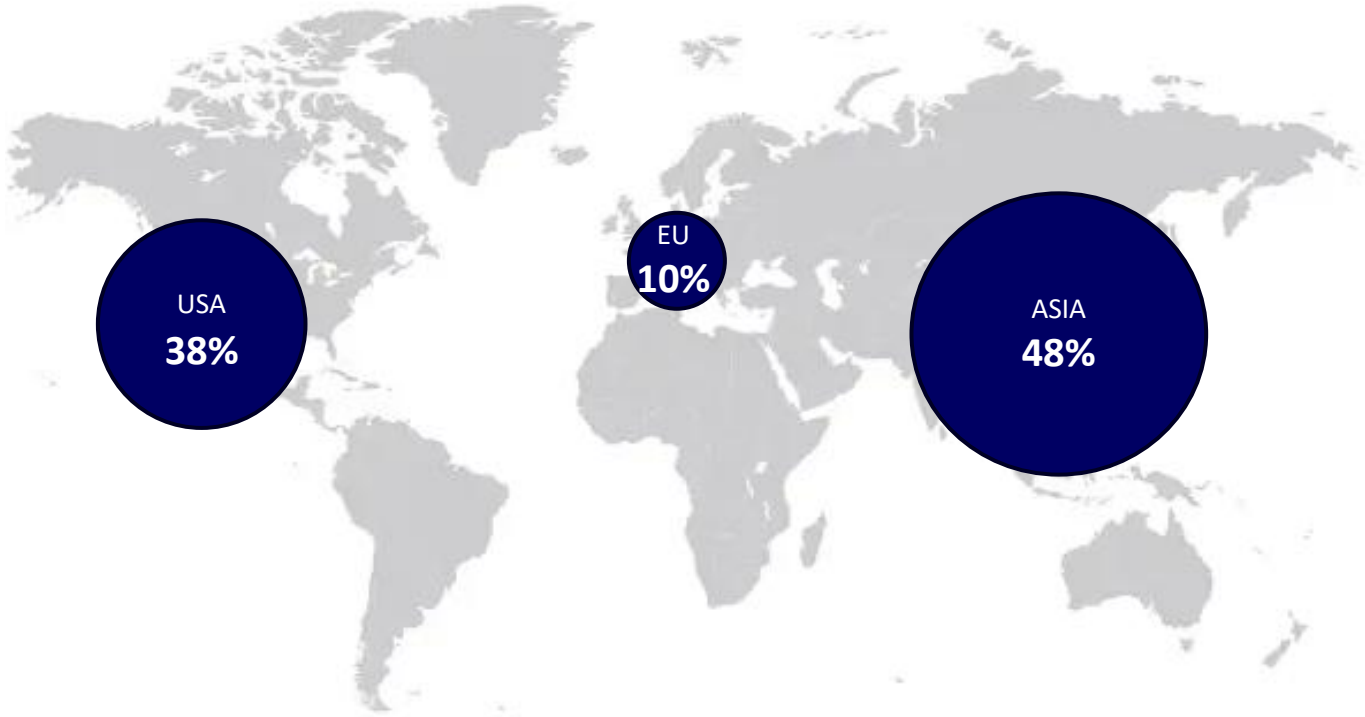
CHIPNL Competence Centre

Opening and welcome

Presentation: Elly Zwartkruis

source: Novio Experience Museum

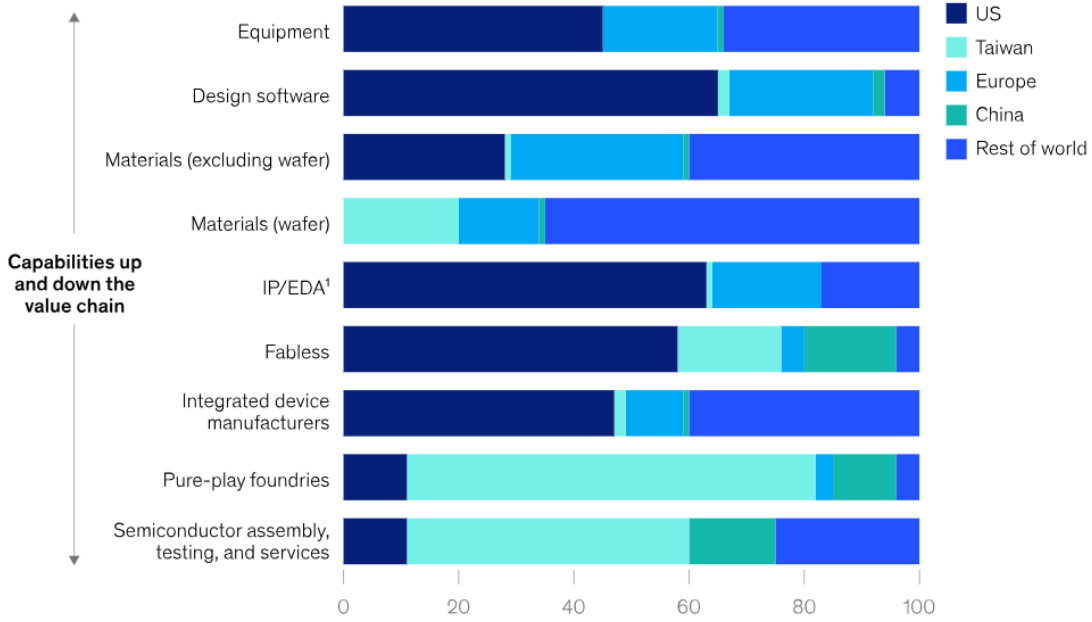
Global market shares*



*source: Silicon Europe 2025

While manufacturing is concentrated in a few locations, other stages of the value chain involve companies in multiple countries.

Sales based on company headquarters location, % share



¹Intellectual property/electronic design automation.
Source: Gartner

Together, we strengthen the position of Europe in the global semiconductor market

Services offered by ChipNL Competence Centre;

- **Supply Chain & Technology**
  - Support for product development, testing and production
- **Business Growth & Funding**
  - Guidance on investment opportunities and growth-related funding programmes
- **Talent & Skills**
  - Access to specialised training, education and matchmaking with industry
- **Promotion & Internationalisation**
  - Boosting visibility and expansion within the European network

CHIPNL Competence Centre

BD – Business Development
PM – Partnership Management
SC – Supply Chain Coordination

Elly Zwartkruis
Managing Director

Rutger Holtzer
Talent Lead

Ron van der Kolk
BD Lead

Vera Janssen
SCC Lead

Peter-Jan Hendrikx
Marcom Lead

Anna Paar
PM – Zuid & West NL

Jeroen van de Put
BD – Zuid NL

Ruben Ottenheijm
Business Intelligence

Nick Hol
Talent – Zuid & West NL

Ivan Stojanovic
BD – Oost & Noord NL

Tasfia Kabir
SCC Photonics

Anneke Bekx
Event Manager

Mark Luke Farrugia
PM – Oost & Noord NL

Albert Vullers
BD – West NL

Judith van der Ven
Marcom Manager

Wouter van Kooten
Talent – Oost & Noord NL

Jacqueline Schardijn
BD – West NL

Thiago Raddo
SCC Electronics

Natasja Thaels
Marcom Manager

Marieke Vizee
Marcom Manager

Bart van ‘t Ende
Investment Mgr

CHIPNL Competence Centre

Introduction: Design Platform

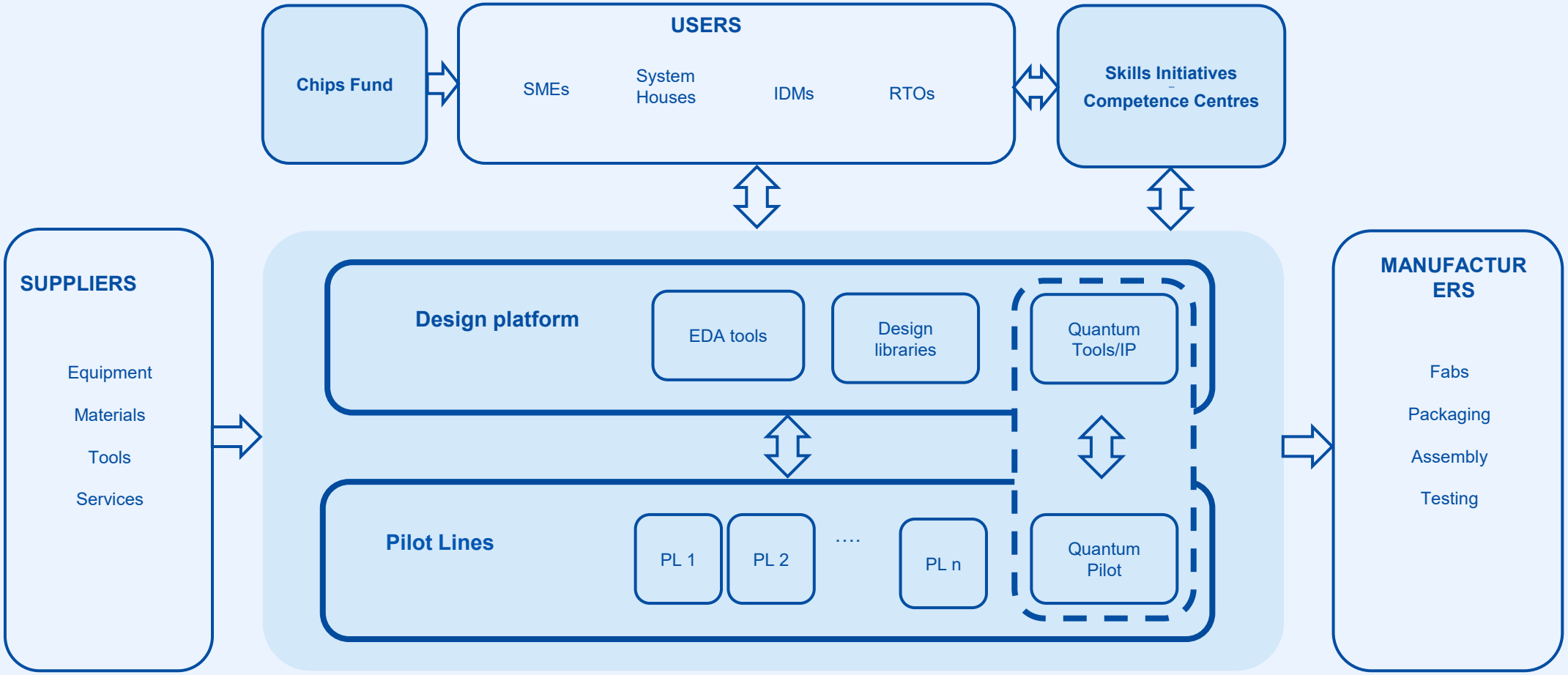
Romano Hoofman

EuroCDP
EU Chips Design Platform

EU Chips Design Platform

Launch event of ChipNL Competence Center
Nijmegen, 29 October 2025

Positioning of the Design Platform

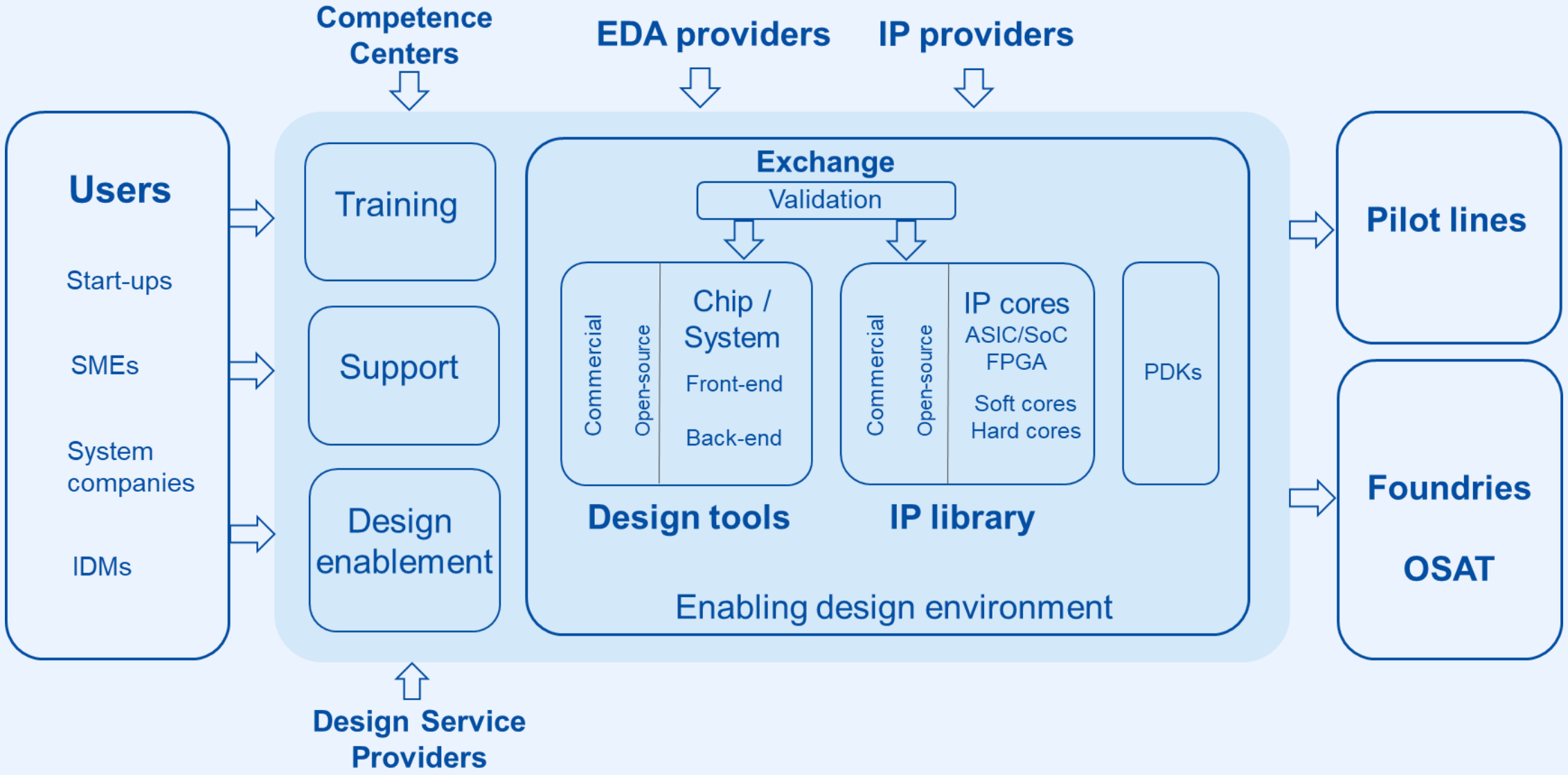


Objectives set by the EC

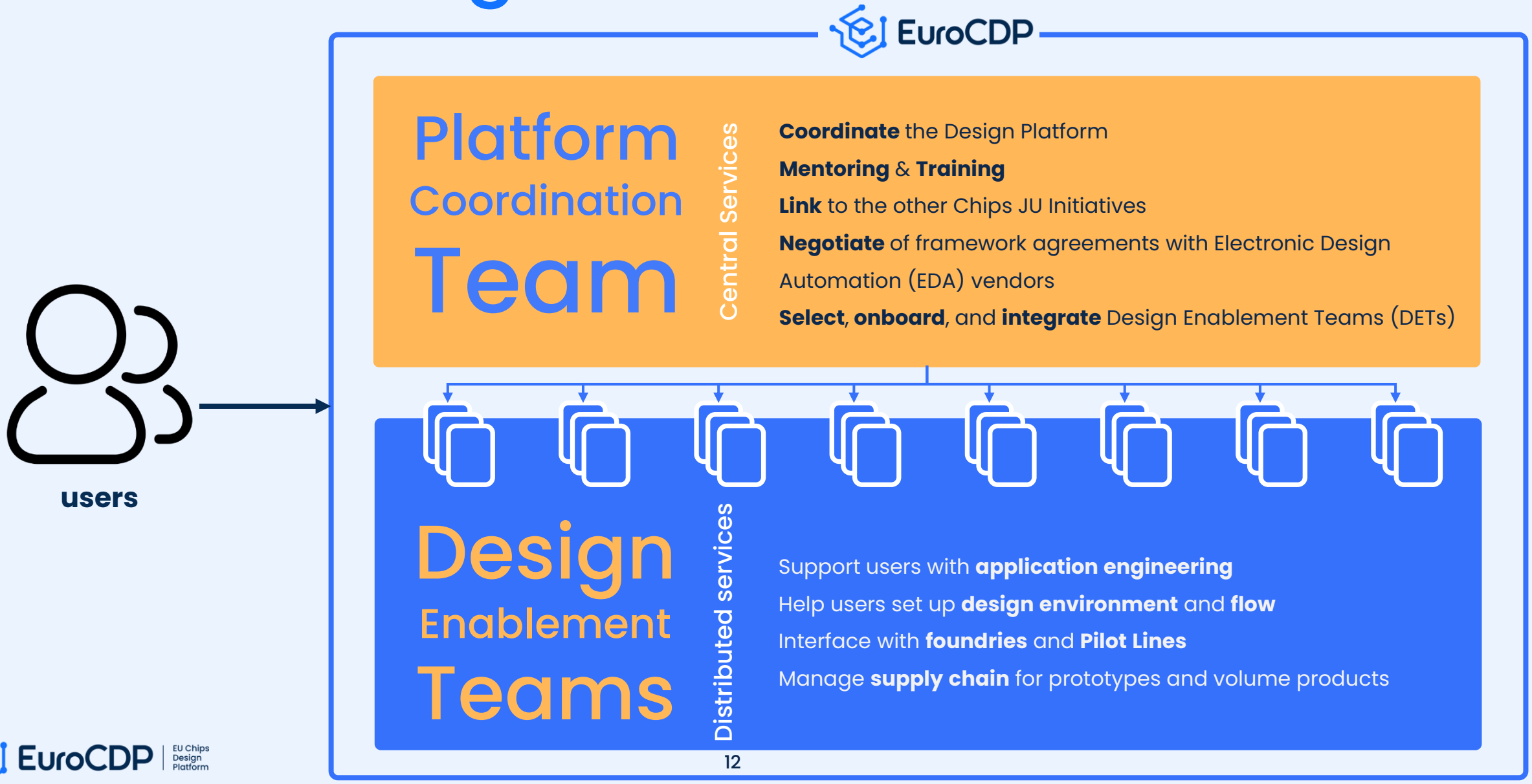
- Lower the barriers for IC design (in particular for adv. tech.)
- Foster collaboration among EU stakeholders
- Support the development of IC design skills by offering training and support services through a network of competence centers
- Integrate access to pilot lines and fabs for early prototyping
- Leverage and build upon existing platforms or initiatives.

Develop a cloud-based design infrastructure where design tools, kits and flows, IP libraries and support services are easily accessible

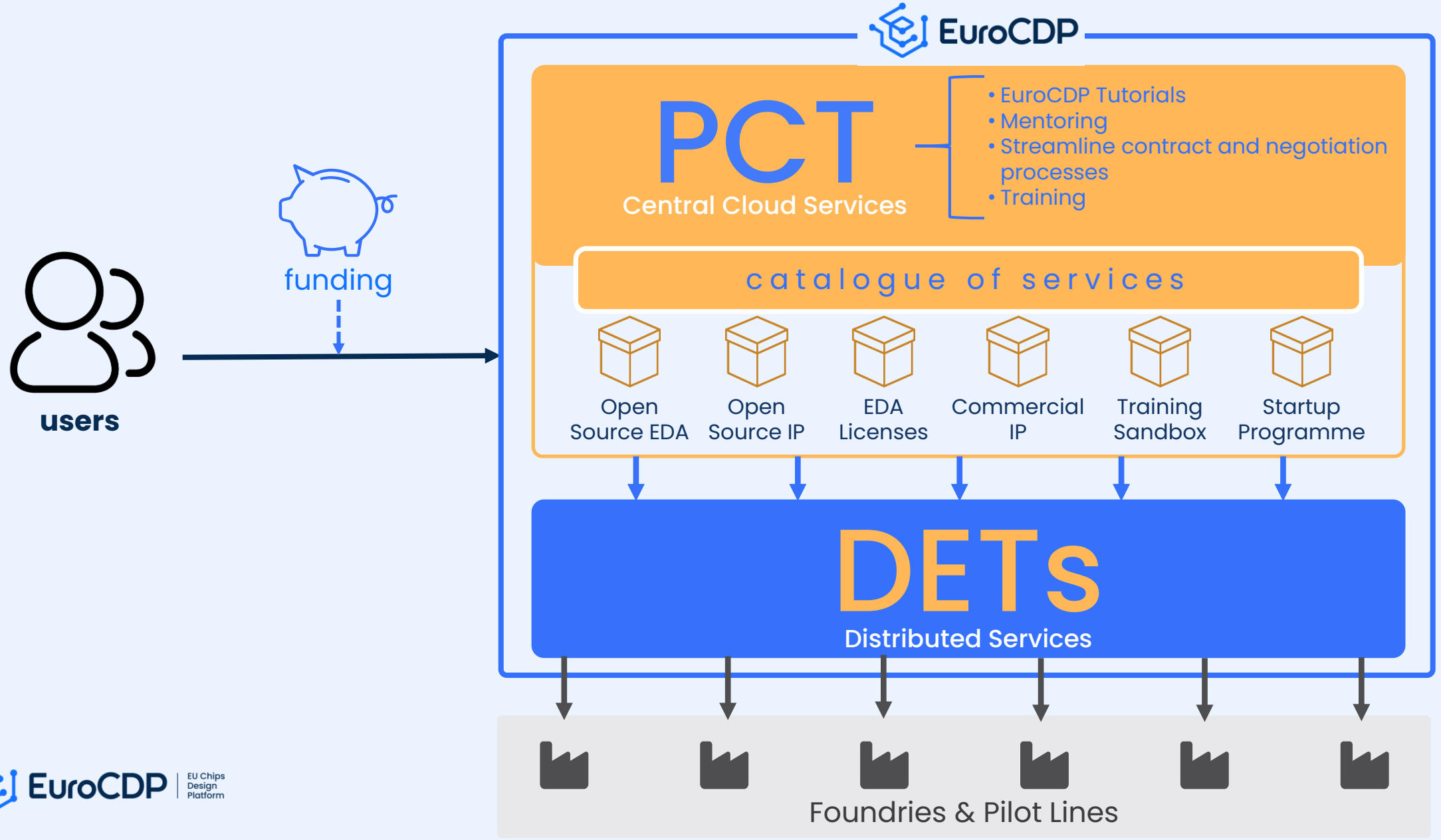
Concept


Competence Centers
EDA providers
IP providers
Users
Start-ups
SMEs
System companies
IDMs
Training
Support
Design enablement
Exchange
Validation
Commercial
Open-source
Chip / System
Front-end
Back-end
Design tools
Commercial
Open-source
IP cores
ASIC/SoC
FPGA
Soft cores
Hard cores
IP library
PDKs
Enabling design environment
Pilot lines
Foundries
OSAT
Design Service Providers

EuroCDP at a glance



EuroCDP architecture



EuroCDP user journey

Fabless use-case

CHIP DESIGN JOURNEY

Industrial solution

central cloud

EDA framework | IPs | Manufacturing | Tests | Debug

Pathfinding	Design	Prototyping	Ramp-up	Production
Ideation	Design flow	MPW shuttles	Private shuttles	Scalability
Training	Expertise	Assembly	Qualification	Operational support
Sandbox	IP sourcing	Test	Supply Chain	Secure Supply Chain
EuroCDP + CCC	EuroCDP			DETs

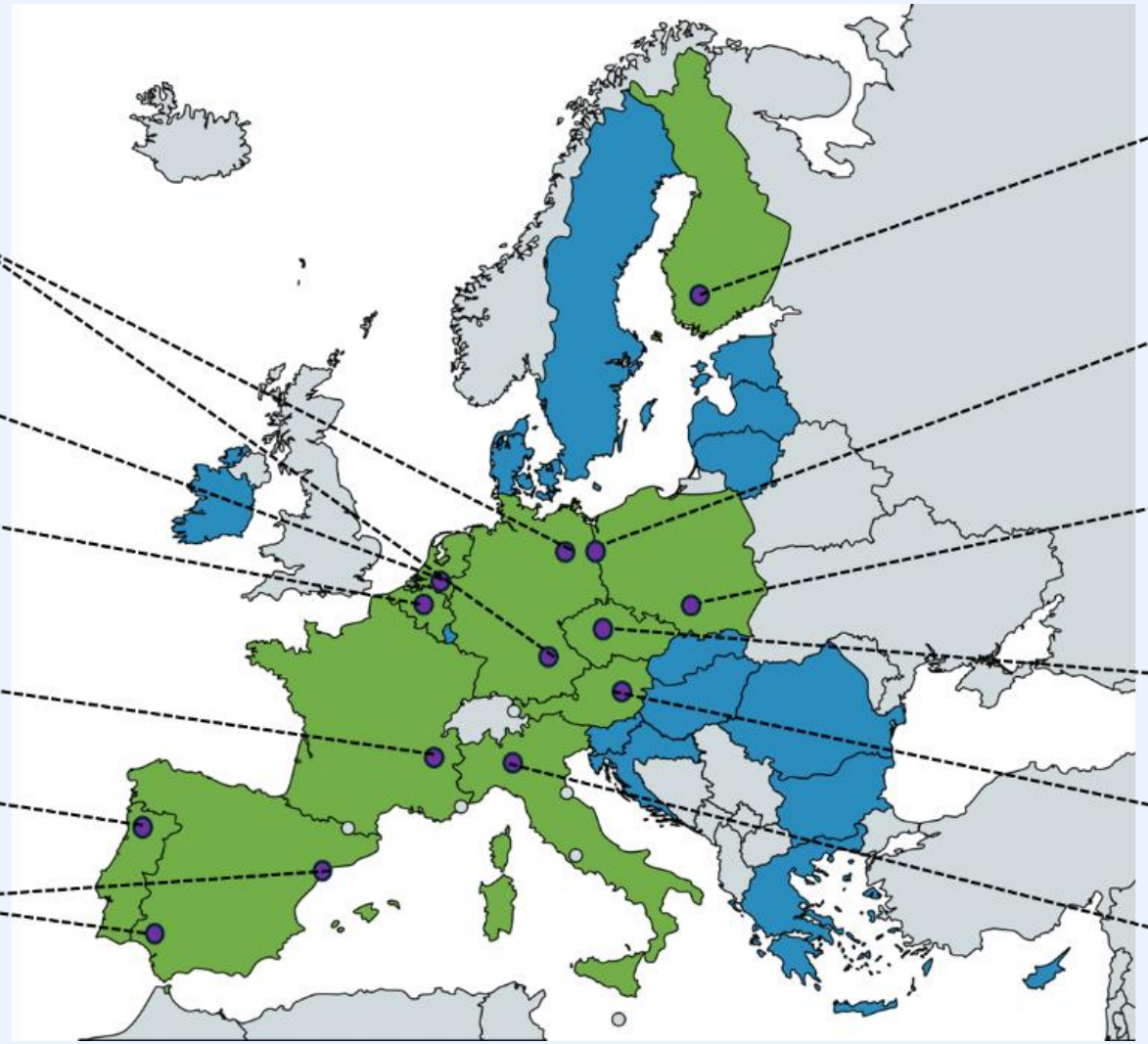
incubation — acceleration

orientation program — startup programs — product and volume

EuroCDP | EU Chips Design Platform

Platform Coordination Team

The PCT consortium



Fraunhofer

TU/e EINDHOVEN UNIVERSITY OF TECHNOLOGY

imec

cea

INL INTERNATIONAL IBERIAN NANOTECHNOLOGY LABORATORY

CSIC CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS

Tampere University

ihp

AGH

ČVUT ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE

SAL SILICON AUSTRIA LABS

Chips-IT

Concept

- Pillar 1: Central cloud to manage services helping fabless companies to innovate and grow.
- Pillar 2: Startup programs to enhance fabless company skills.
- Pillar 3: A distributed network of heterogeneous Design Enablement Teams (DET) to provide design and manufacturing services tailored to individual company needs.
- Pillar 4: Pre-defined licensing agreements of commercial EDA tools and IPs to significantly reduce the time required for fabless companies to get access.
- Pillar 5: Various levels of support to guide fabless companies throughout their journey.

Startup programs

MENTORING

- Business and technical
- Freely accessible for all selected users
- Mentor network of semiconductor industry experts
- Experts are available on a specific schedule («office-hours») or «on-call»
- EuroCDP handles mentoring requests and connects SMEs with the most suitable mentor

INCUBATION

- Free-running program
- Mentoring activities accessible as for ←Mentoring
- Dedicated training material (entrepreneurship, go to market, etc..) accessible from an on-demand library

ACCELERATION

- Equity free
- Cohort based program (min. 2 cohorts per year – max 6-10 startups per cohort)
- Compulsory frontal courses and mentoring activities from industry leaders and entrepreneurs (on-site 2 week program)
- Setting of KPIs and goals for startup «graduation»
- Continuous mentoring to check on KPIs and goals
- **Demo-day** pitch in front of VCs, exhibition boots and «graduation» ceremony

EuroCDP | EU Chips Design Platform

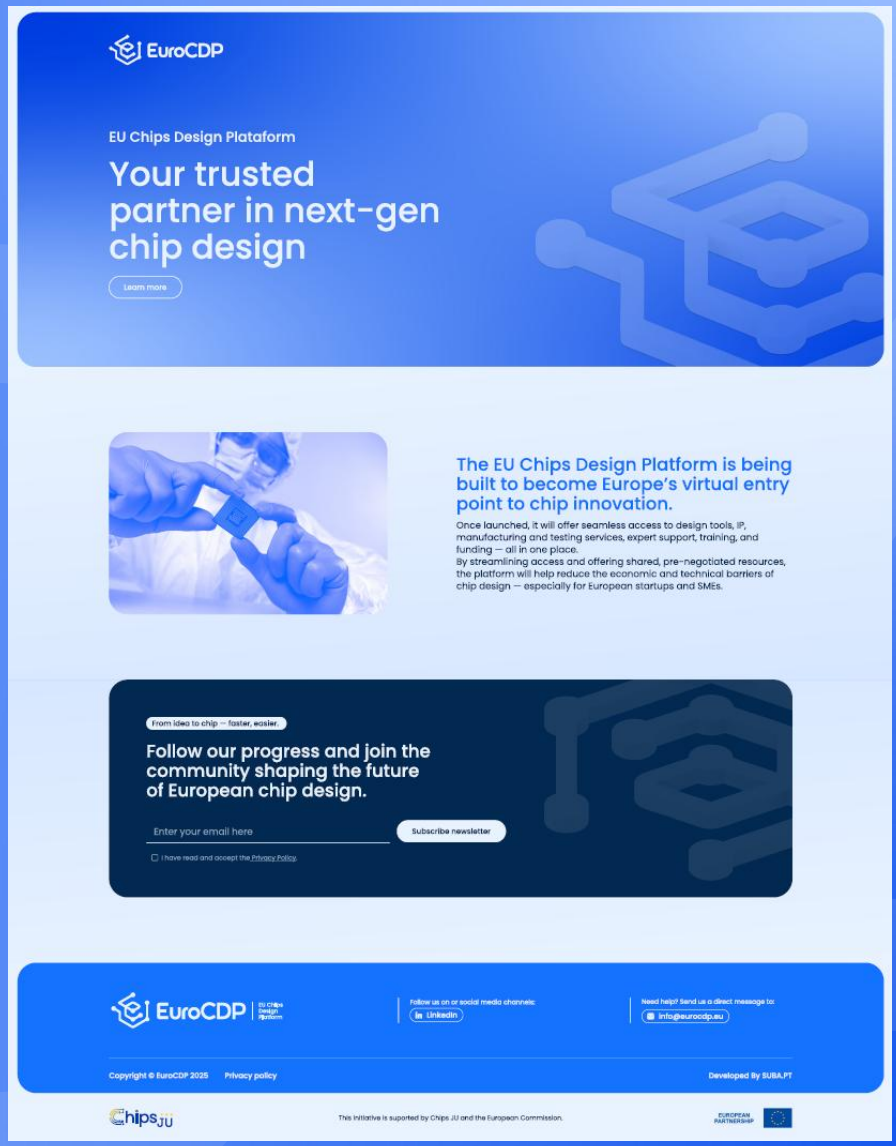
Interactions with CCCs

Startups/SMEs from CCCs to EuroCDP

Early Engagement **Technology Discovery** **Project Development**

EuroCDP | EU Chips Design Platform

Stay in touch with us!



EuroCDP

EU Chips Design Platform

From idea to chip — faster, together.

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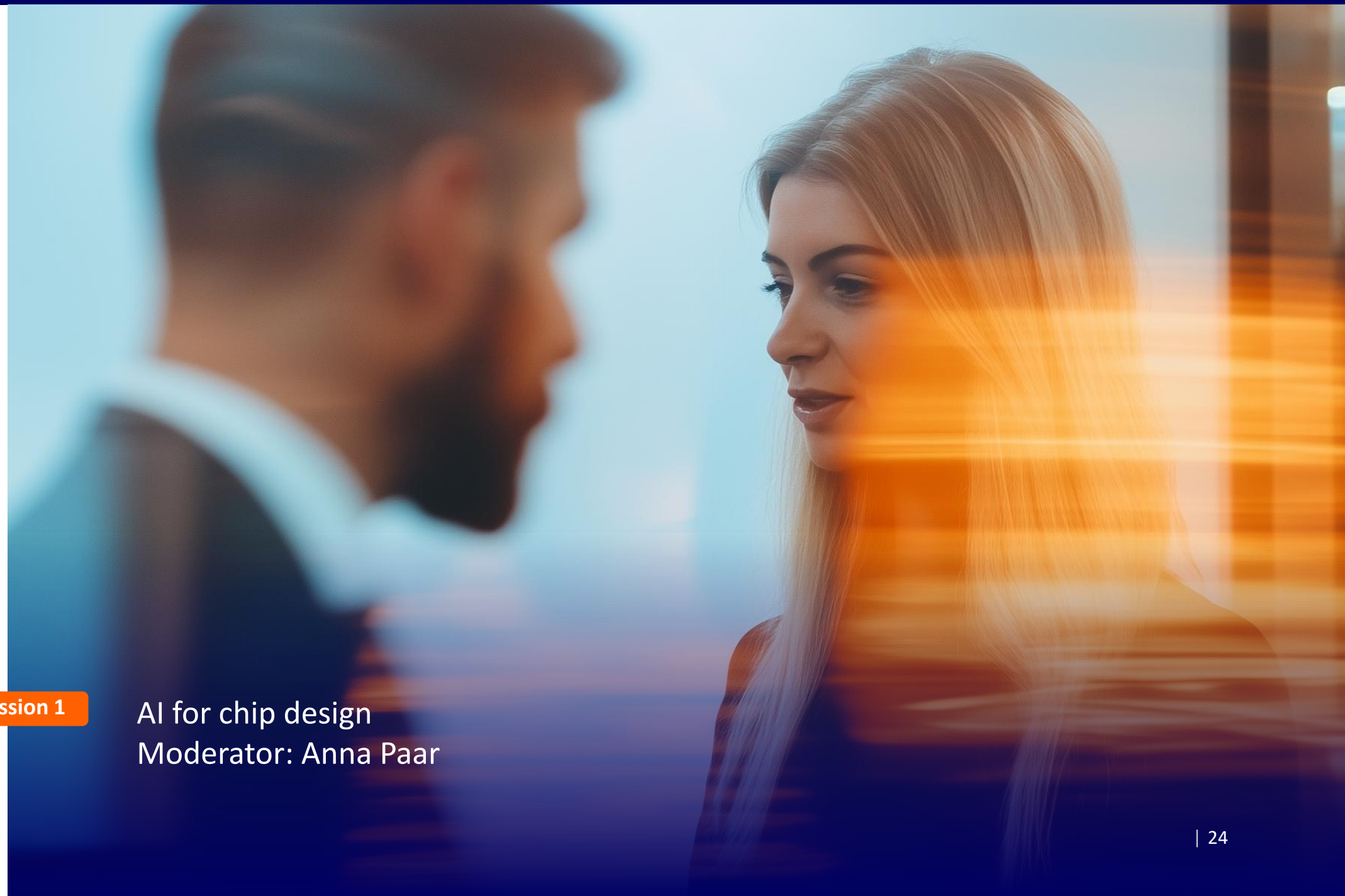
Deep dive: Chip Design

Bratislav Tasic

CHIPNL Competence Centre



Panel Discussion 1

AI for chip design

Moderator: Anna Paar

CHIPNL Competence Centre

If chip designers are replaced by AI, how should we respond?

Panellists

Aida Todri-Sanial
TU/e
Full Professor Integrated Circuits

Bratislav Tasic
NXP
Department and Program Manager

Christiaan Baaij
QBayLogic
Co-Founder

Giuseppe Garcea
Axelera AI
Co-founder and R&D director

CHIPNL Competence Centre

Deep dive: Heterogeneous Integration

Martijn Heck

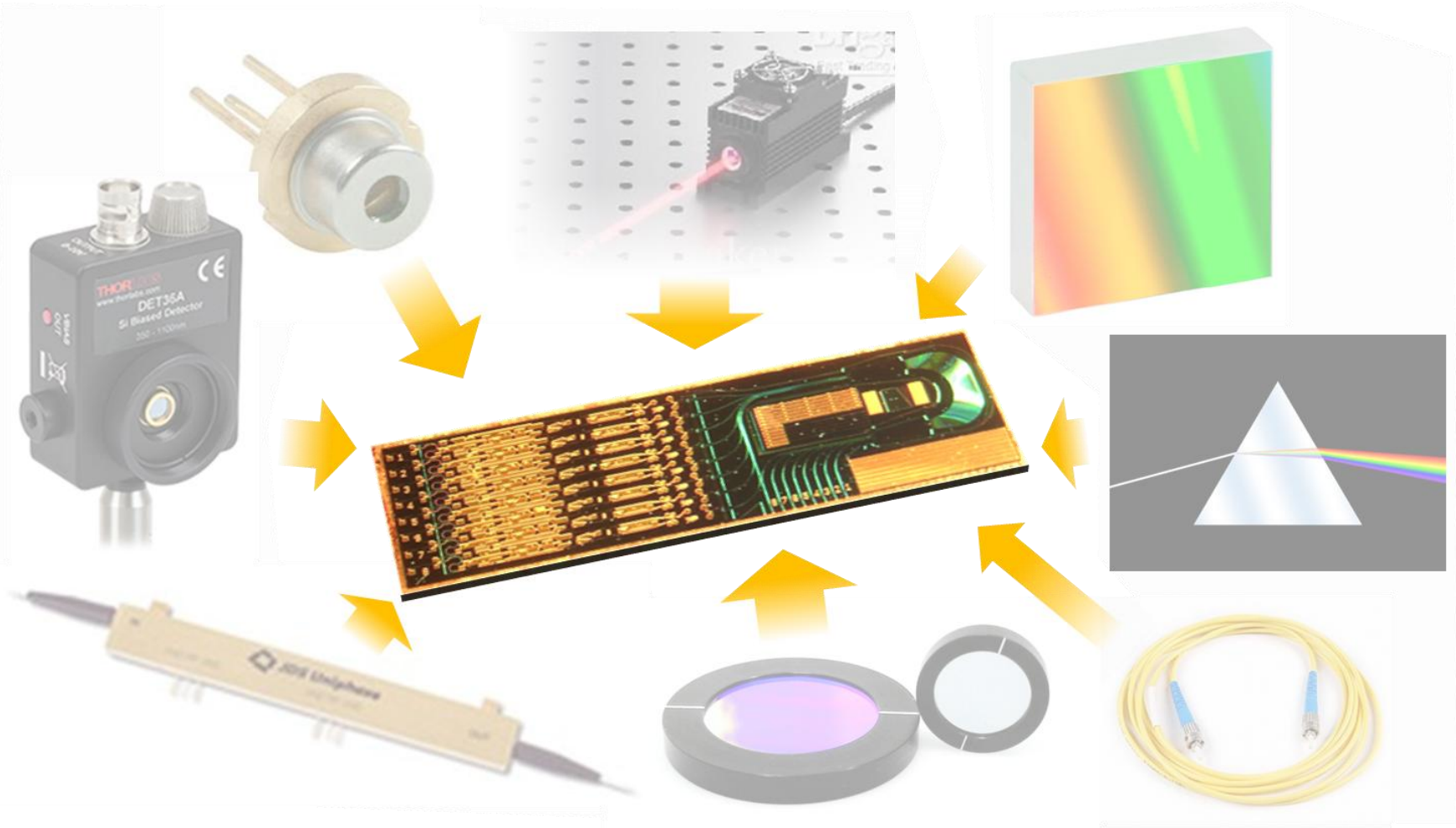
The interaction between semicon and photonics

October 29. 2025, Launch ChipNL Competence Centre, Nijmegen

Martijn J. R. Heck

Department of Electrical Engineering, Photonic Integration

Photonic integration: optical chips



A **photonic integrated circuit** combines various optical components, such as waveguides, lasers, detectors, modulators, filters and multiplexers, on a single substrate. This is done using technologies and processes developed in the semiconductor industry.

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Advantages of photonic integration

increased performance

in terms of stability, speed and sensitivity, improves electronics performance;

decreased size, weight and power (SWaP)

for use in, e.g., drones, space and aircraft, handheld and wearable devices;

decreased cost

at high volumes due to wafer-scale manufacturing.

100 Gbps transmitter
R. Nagarajan, Infinera, 2006

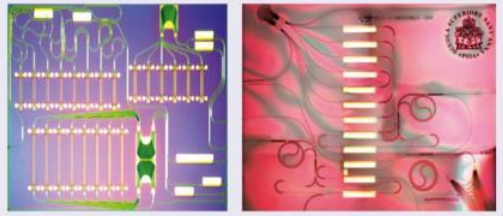
The ecosystem

JePPIX Knowledge JePPIX MPW Services JePPIX Pilot Line

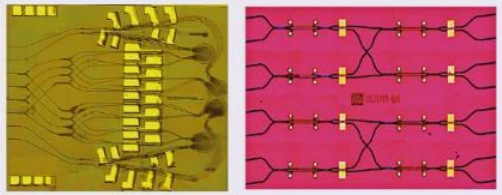
Over 1000 PIC designs realised in JePPIX foundries

THz and RF circuits

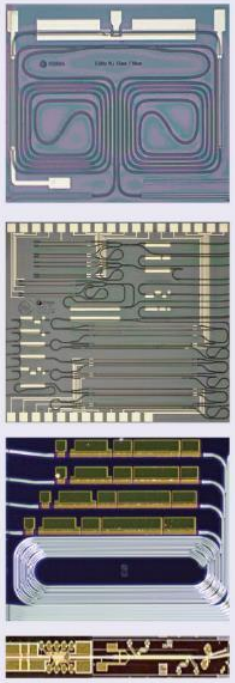
Optical data handling



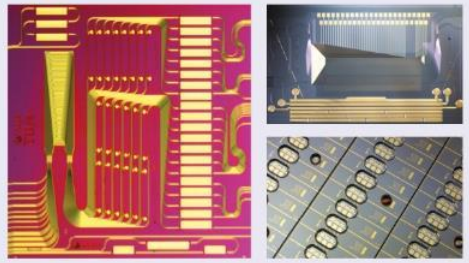
Optical switching



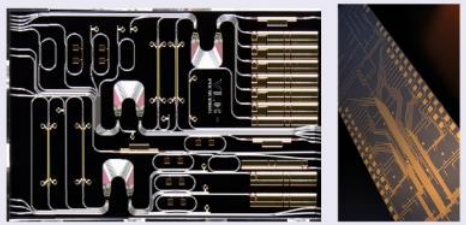
Variety of Lasers



Medical and bio-imaging

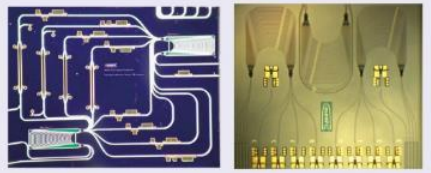


Microwave photonics beam-former

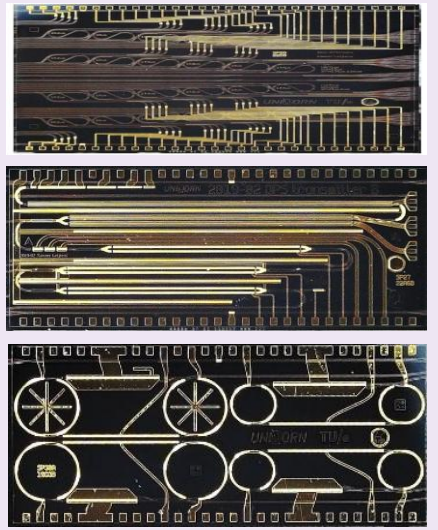


Sensor readout units

Fibre to the home



QKD transceivers



New pilot line services launched with manufacturing-grade PDKs and test automation

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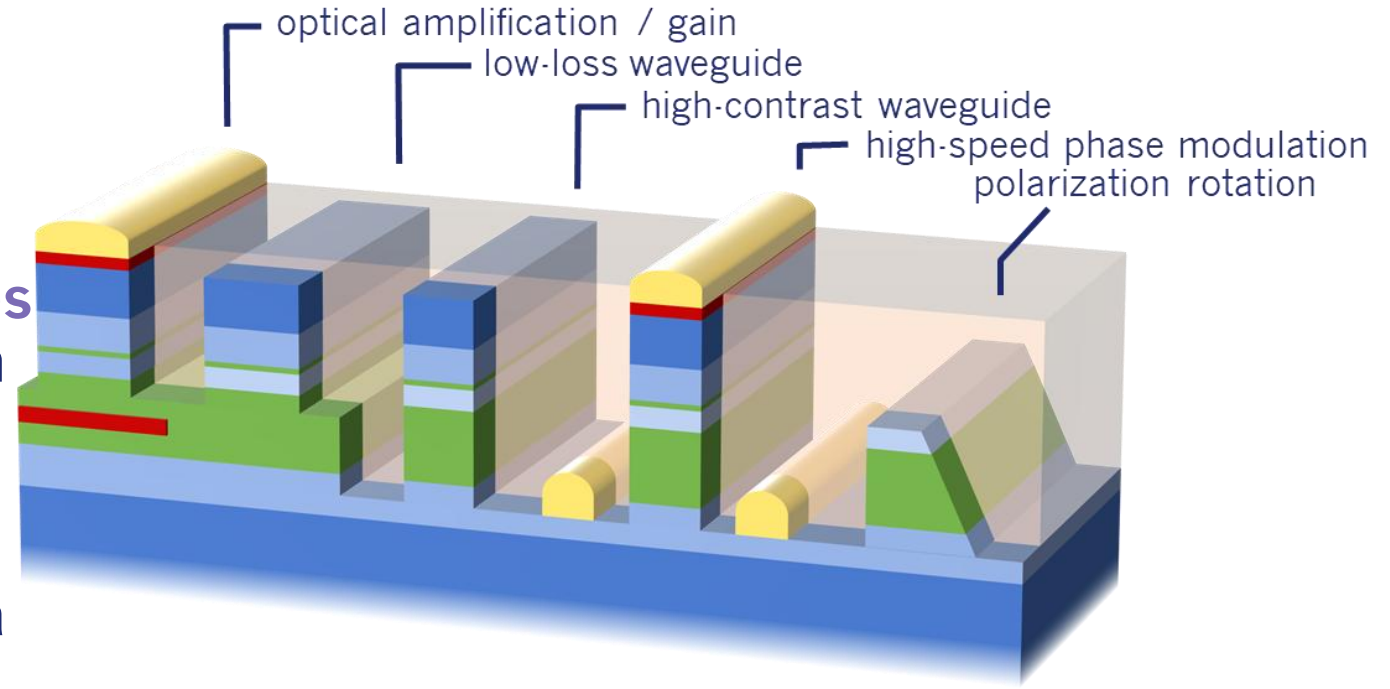
JePPIX
Platform for Photonic Integration

Drives the use of indium phosphide, silicon nitride and hybrid photonic integration

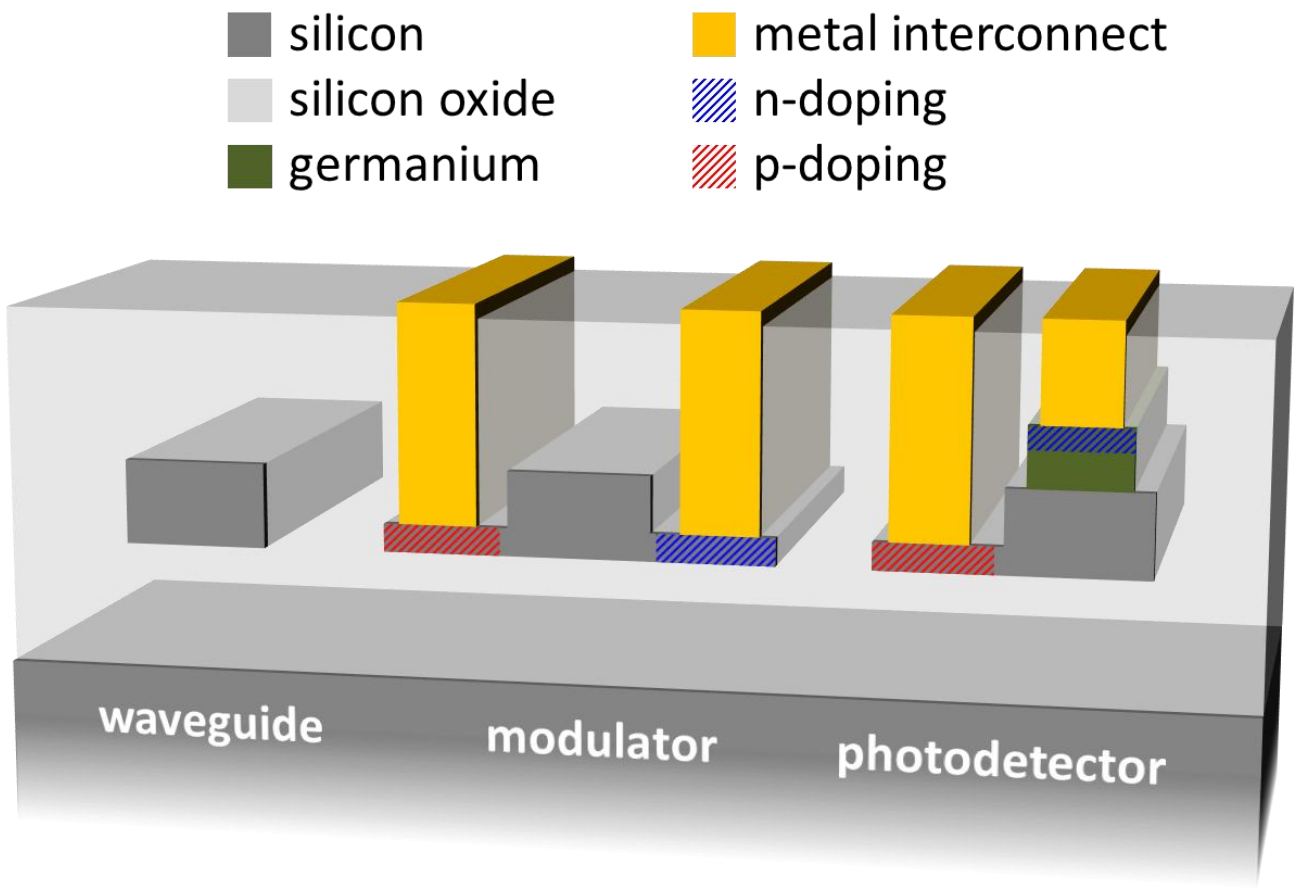
JePPIX Pilot Line offers industry a path to manufacturing;

JePPIX Multi-Project Wafer Services offers academia and industry a path to prototyping;

JePPIX Knowledge supports education and training for academia and industry.



Silicon photonics: CMOS compatible nanophotonics



Silicon photonics uses CMOS-compatible technologies and processes – or even a CMOS process – to create a photonic integrated circuit. Waveguides, modulators and photodetectors are available for 50 Gbps. External lasers are required.

“Groeimarkten voor Nederland” – Min. Economic Affairs

Tabel 1: Lijst van geïdentificeerde kansrijke groeimarkten voor Nederland

Hoofdmarkt	Deelmarkt
Halfgeleiders	• Analoge microchips • Fotonische microchips
Machinebouw	• Chipmachines • Machines voor de agrifood-sector
Quantumtoepassingen	• Quantumcomputers, -componenten (i.h.b. koelingselementen) en quantumsoftware • Quantumcommunicatie • Quantumsensoren
Innovatieve chemie	• Geavanceerde chemie • Circulaire en biobased materialen • Nieuwe generatie biobrandstoffen

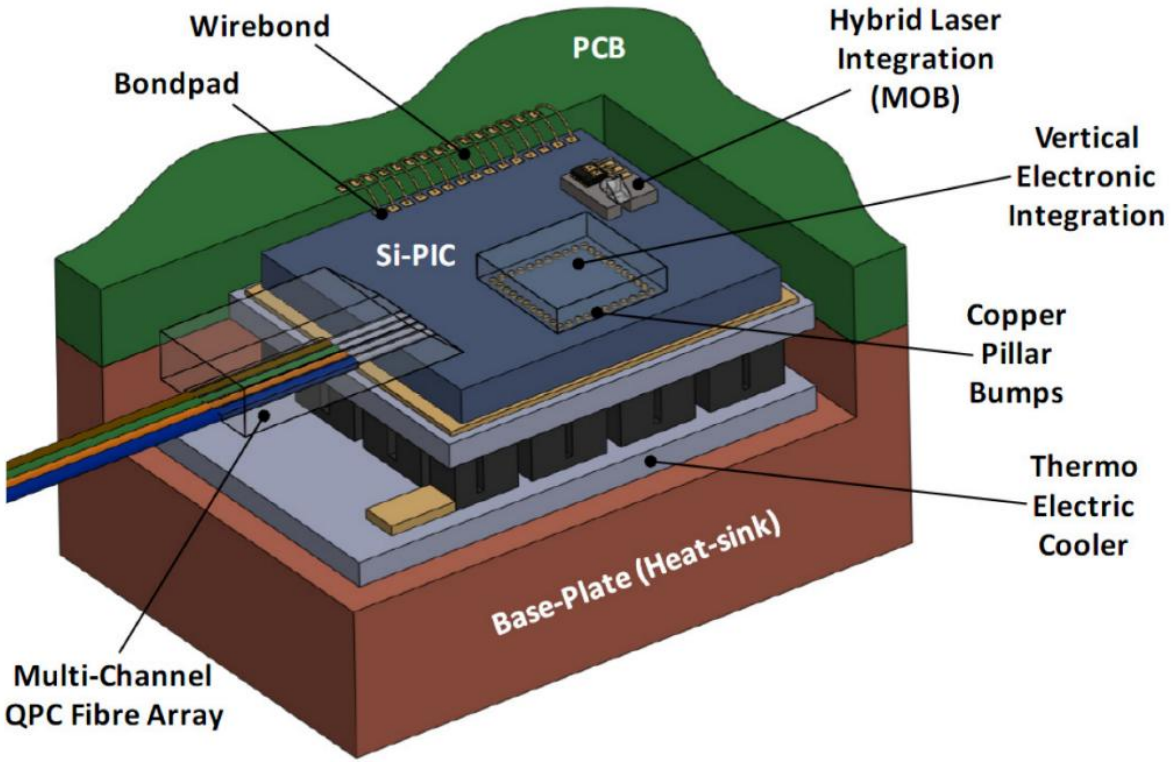
Why the synergy electronic-photonic?

- Same or similar **manufacturing**, same or similar fabs
- Converging electronic-photonic **design** automation
- Increasingly overlapping **talent** pipeline
- Joint **application** space
    - PICs need ICs for drivers, control, signal-processing, memory, …
    - ICs (might) need PICs for communications, microwave technology, sensing interfaces, …

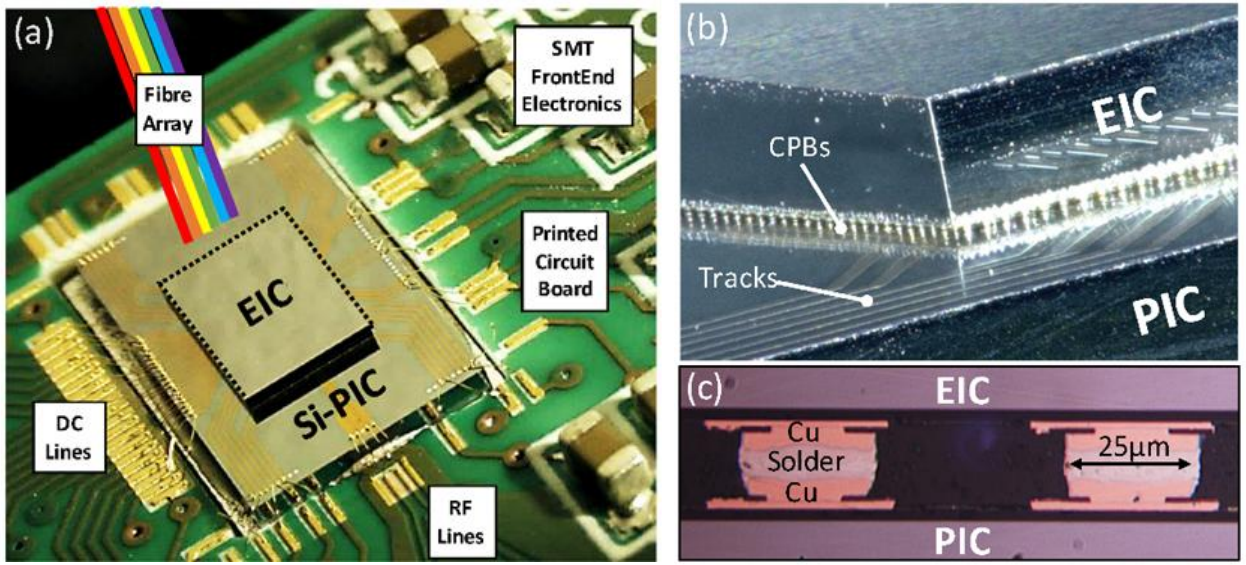
→ need and opportunities for **heterogeneous integration** techniques

HOW CAN WE INTEGRATE ELECTRONICS AND PHOTONICS ON AN INTEGRATED CIRCUIT?

Electronic-photonic integration of separate dies: copper pillar bump bonding

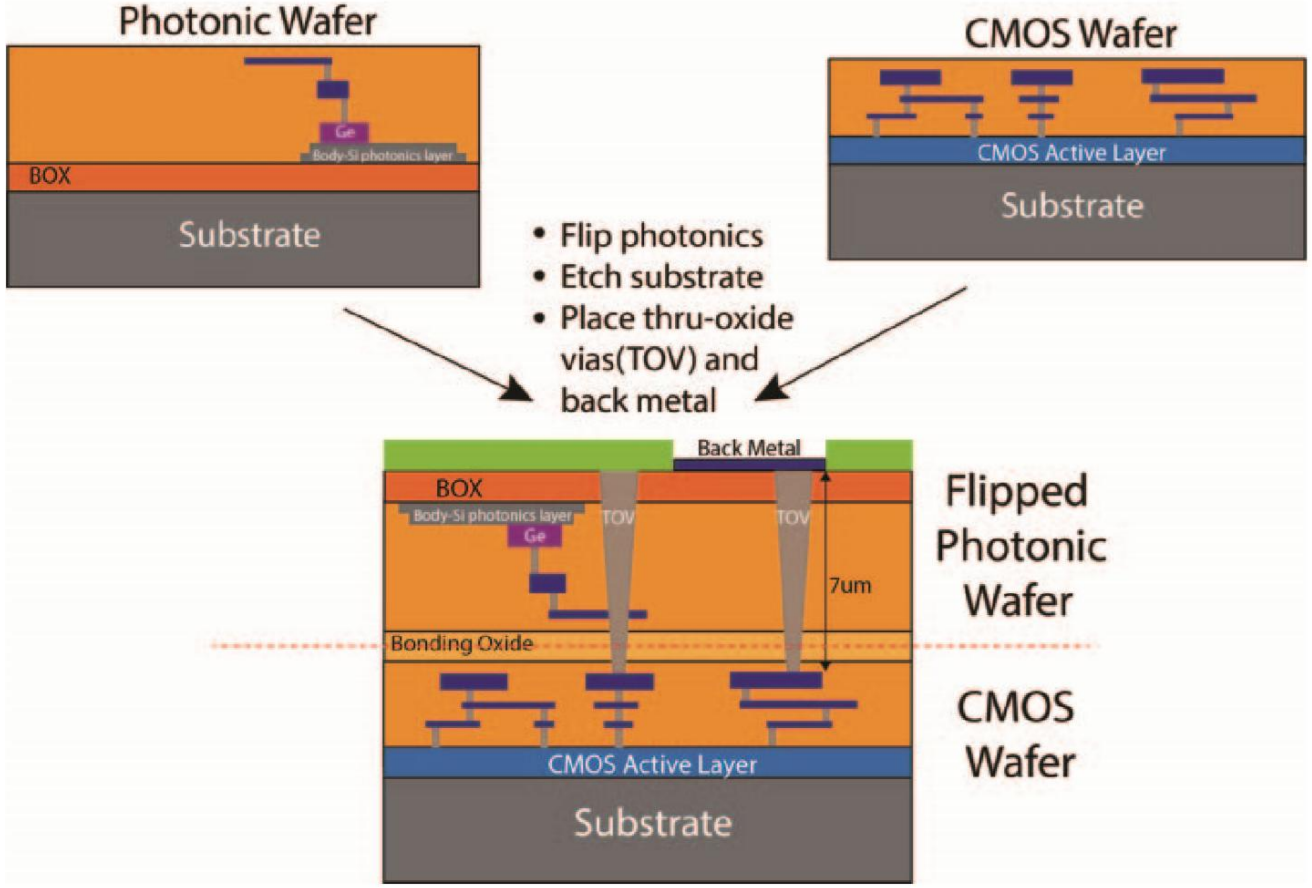


Electronic IC dies are flipped and bonded face-to-face on the photonic IC die by thermo-compression bonding of copper pillars, thereby forming dense and short electronic connections.



L. Carroll, Appl. Sci. 6, 12 (2016)

Waferscale electronic-photonic integration: through-oxide vias



Full wafers are bonded face-to-face and the substrate of the photonic wafer is removed. Electrical connections are then made by etching holes through the top photonics wafer and into the electronics wafer, and filling these with metal, so-called through-oxide-vias.

N. DiLello Heidel, IEEE JSTQE, 22, 6 (2016)

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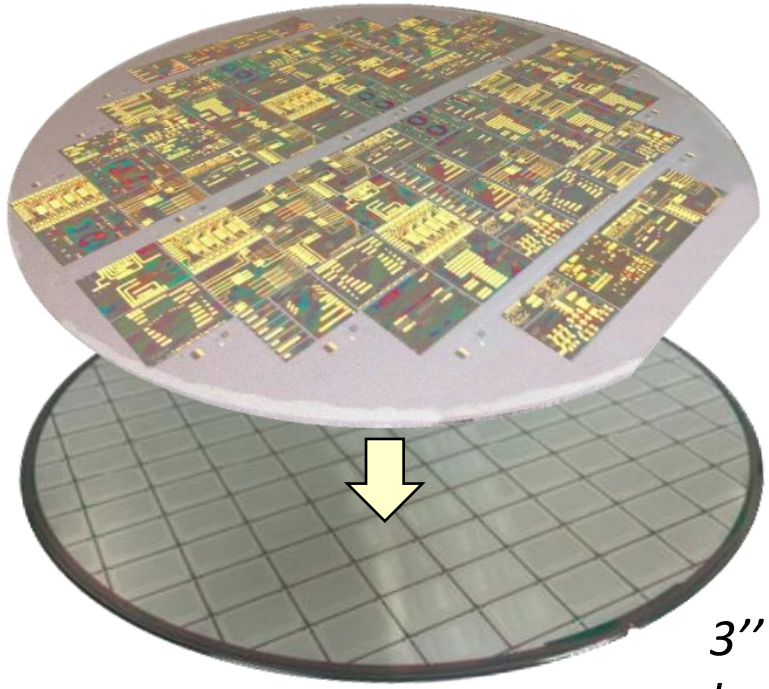
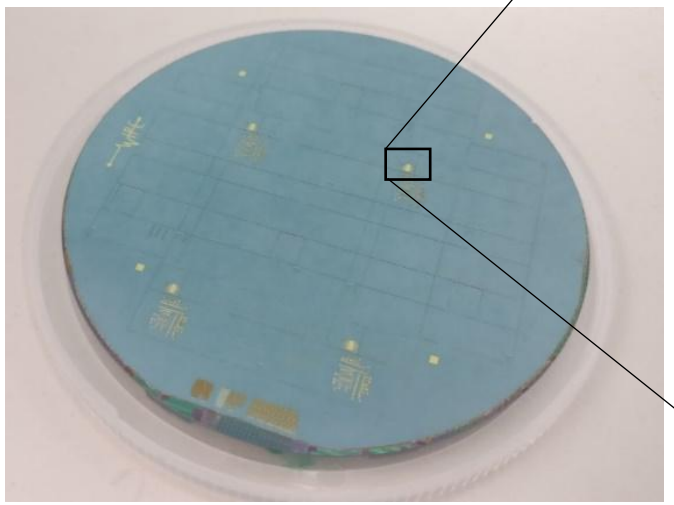
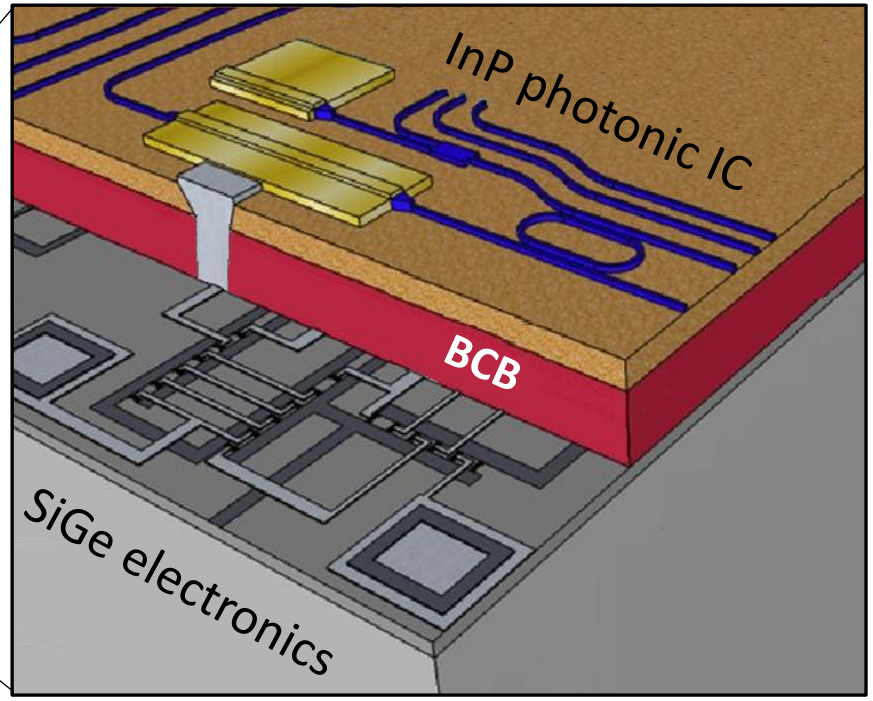
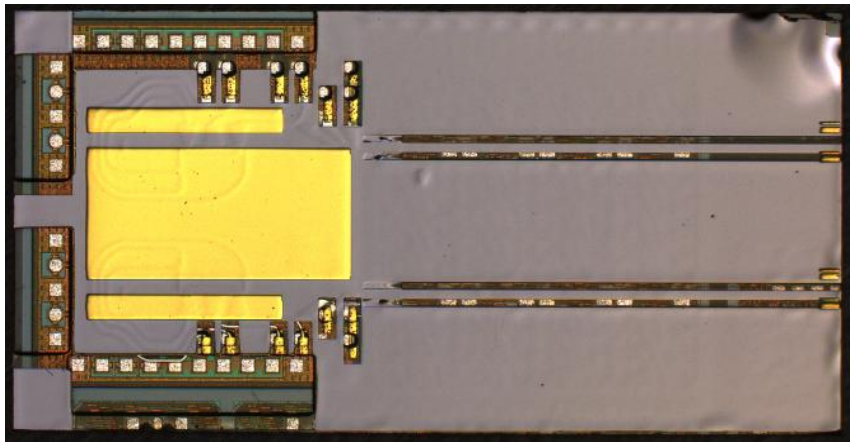
Waferscale electronic-photonic integration with InP







3'' InP PIC wafer from HHI bonded to laser-sawn BiCMOS wafer from NXP



Intimate co-design to remove components and parasitics

Systematically improve efficiency, speed, and information density

Using wafer scale processes

PHOTONICS PUBLIC PRIVATE PARTNERSHIP

http://wipe.jeppix.eu

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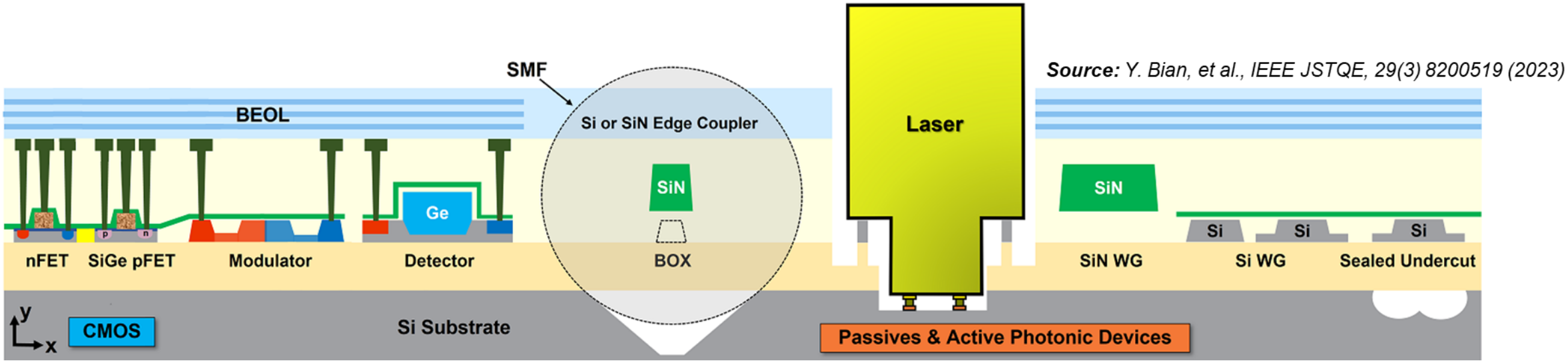
Global Foundries' GF Fotonix

- Monolithic integration of Photonic Devices with a 45nm class RFCMOS
- 65-GHz photodiodes, 50-GHz modulators, 100-GHz TIA



https://gf.com/technology-platforms/silicon-photonics/

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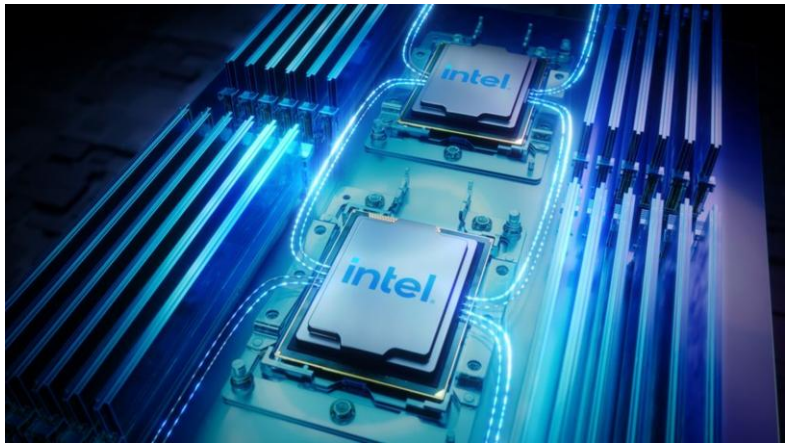
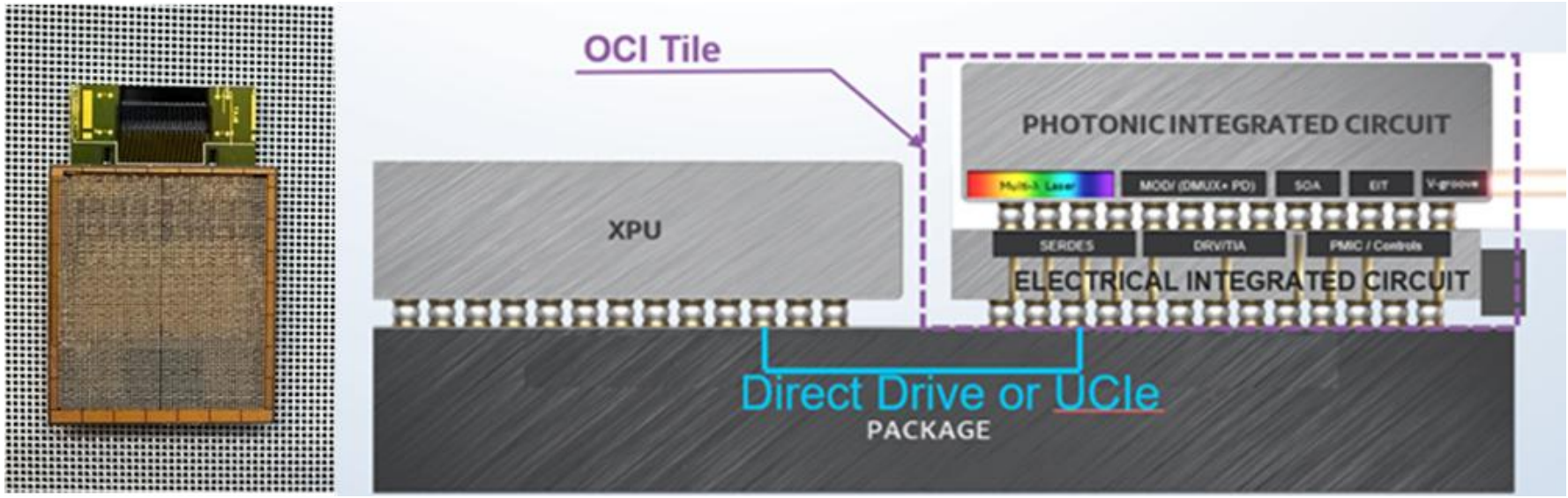
Intel – Optical Compute Interconnect (OCI) chiplet



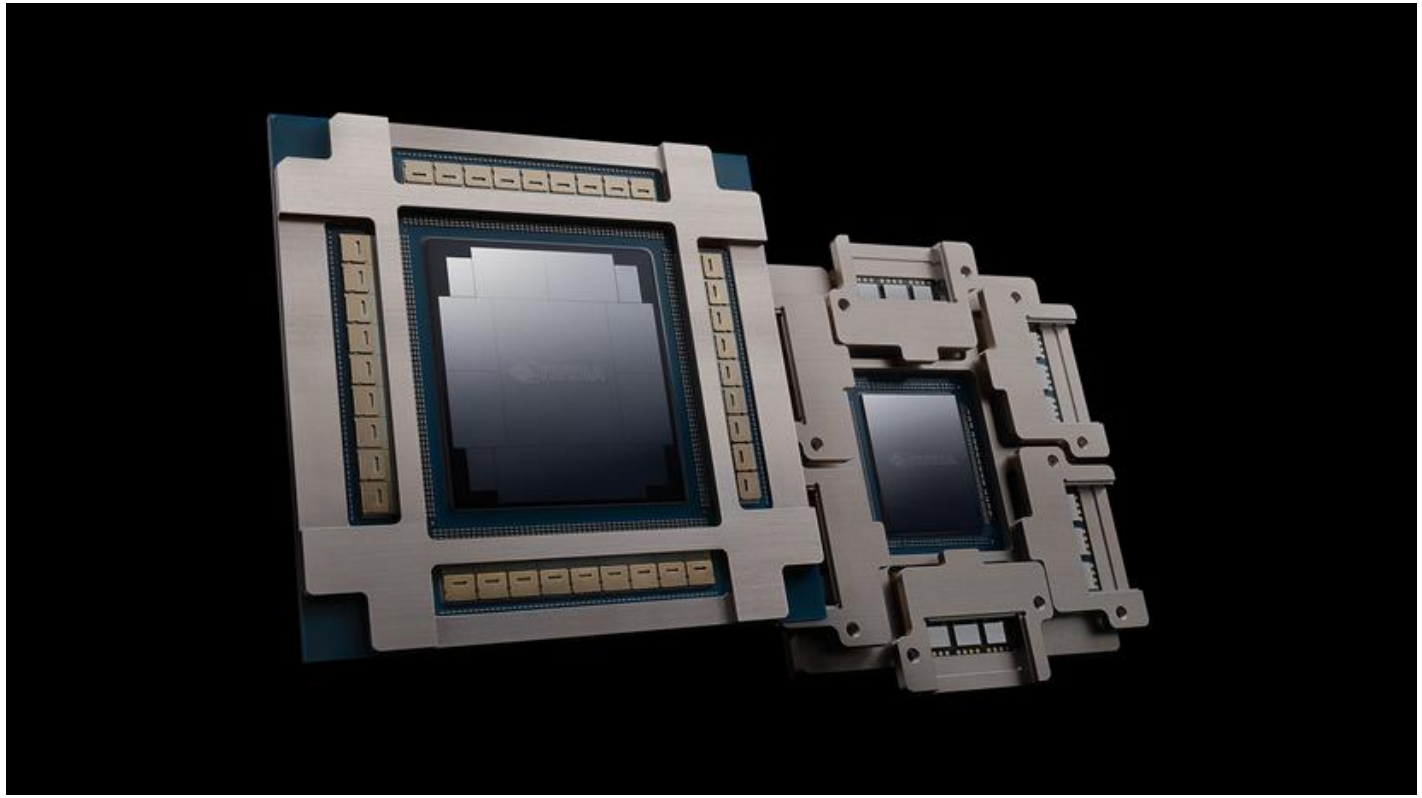
Intel 4 Tbps Optical Compute Interconnect (OCI) Chiplet

https://community.intel.com/t5/Blogs/Tech-Innovation/Artificial-Intelligence-AI/Intel-Shows-OCI-Optical-I-O-Chiplet-Co-packaged-with-CPU-at/post/1582541



NVIDIA Spectrum X Photonics – co-packaged optics

- connect millions of GPUs in AI factories
- silicon photonics
- 3.5× better energy efficiency
- enabling 100-400 Tbps total bandwidth



https://nvidianews.nvidia.com/news/nvidia-spectrum-x-co-packaged-optics-networking-switches-ai-factories

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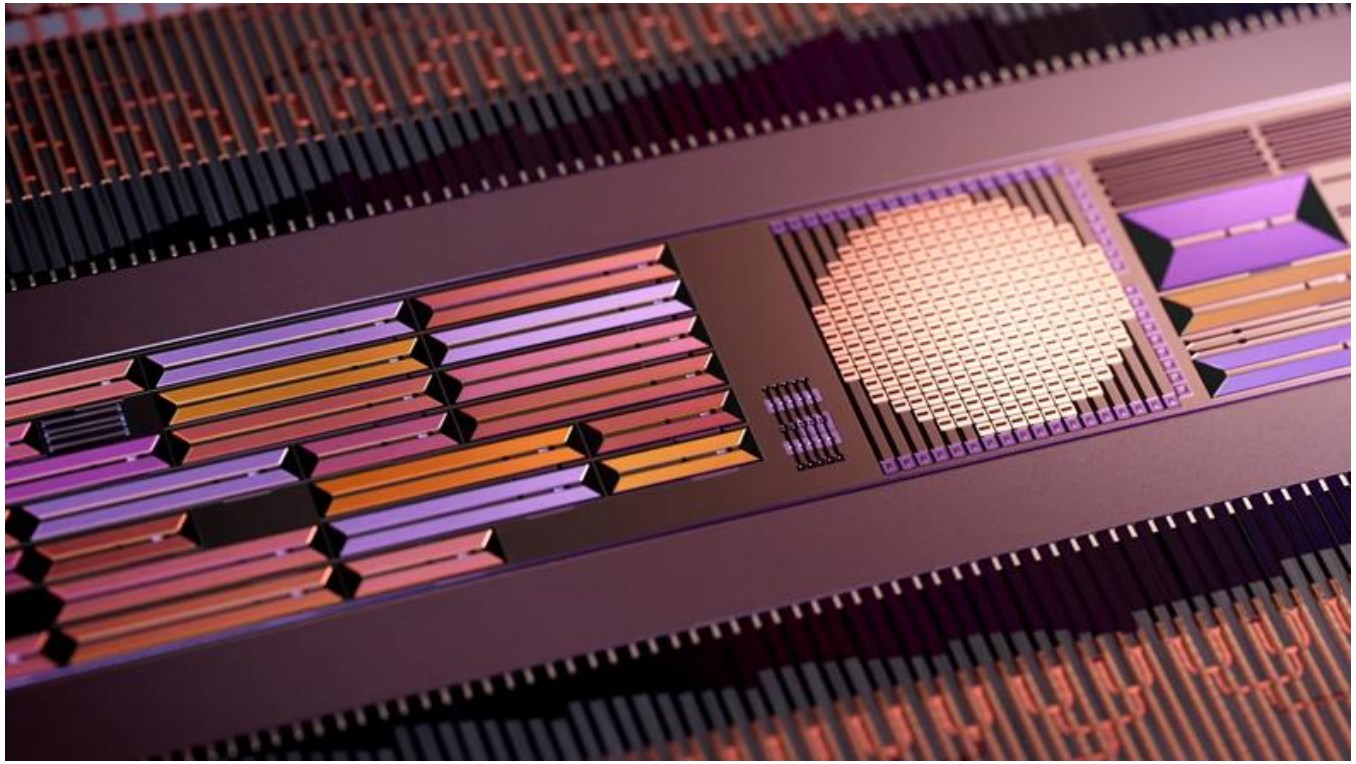
Google's Taara chip – free-space optical communication

- Goal: datacom without fiber…
- for fast, abundant and low-cost connectivity
- silicon photonic optical phased array (OPA)
- 10 Gbps over 1 km



https://x.company/blog/posts/taara-chip/

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That's why the synergy!

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    - ICs (might) need PICs for communications, microwave technology, sensing interfaces, …

Let's discuss the need and opportunities for **heterogeneous integration** techniques for the Netherlands

Martijn J. R. Heck

Department of Electrical Engineering

Eindhoven University of Technology

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https://www.linkedin.com/in/martijnheck/

CHIPNL Competence Centre

Panel Discussion 2

Heterogeneous Integration

Moderator: Martijn Heck

CHIPNL Competence Centre

Towards a succesvol Heterogenous Integration approach based on the Dutch strenghts

Panellists

Sander Roosendaal
Synopsys
Director, R&D Engineering

Jan Leideman
DEMCON
New Business Development Manager

Rob Hendriks
FononTech
CEO & Co-Founder

Willem van Driel
TU Delft
Professor, Chairman

CHIPNL Competence Centre

Panel Discussion 3

Internationalisation Ambitions

Moderator: Naomie Verstraeten

What are the sector's long term internationalisation ambitions?

Panellists

Ben Ruck
Ministry of Economic Affairs & Climate Policy
Programme coordinator European R&D&I

Mark Luke Farrugia
ChipNL Competece Centre
Partnership manager

Toine Cleophas
BOM
Sr Project Management | Foreign Direct Investments

Arian Zwegers
European Commision
Deputy Head of Unit "Microelectronics and Photonics"

CHIPNL Competence Centre

Menti Meter

Your input was highly appreciated and parts were also used for the Public Consultation Chips Act 2.0

The answers on the following 4 slides represent the opinion of various groups, consisting of:

- Start-ups and SMEs
- Supply industry and industrial users
- RTO and academia
- Industry associations and experts
- Government bodies

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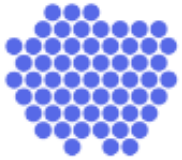
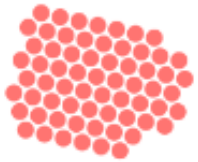
What are they key vulnerabilities in the current semiconductor supply chain?



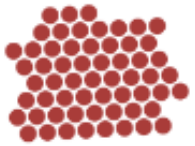
21% Limited production capacity in Europe



23% Geopolitical tensions

0% Logistical challenges

4% Supply chain transparancy



21% Dependence on non-EU suppliers

7% Technology gaps

8% Material scarcity

10% Regulatory barriers

6% Others

16 104

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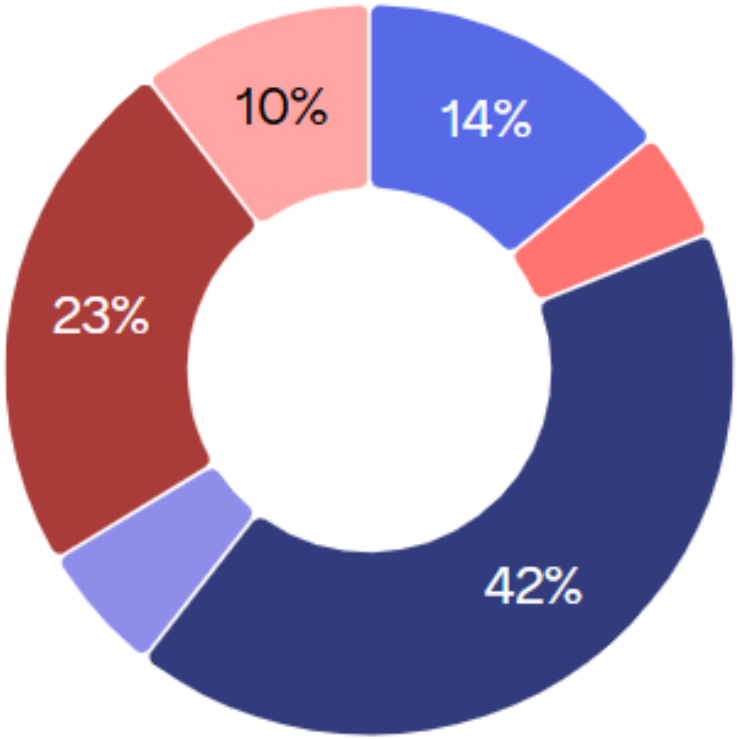
In which segments of the value chain do you think the EU has the potential to gain or to further reinforce its leadership in the coming years?



- 14% Software for chip design
- 5% Basic IP Inputs (materials, chemicals, gases)
- 42% Semiconductor manufacturing equipment
- 6% Manufacturing of Mainstream chips (28 nanometres)
- 23% Packaging, Testing and Assembly of chips
- 10% Manufacturing of Advanced chips (< 10 nanometres)

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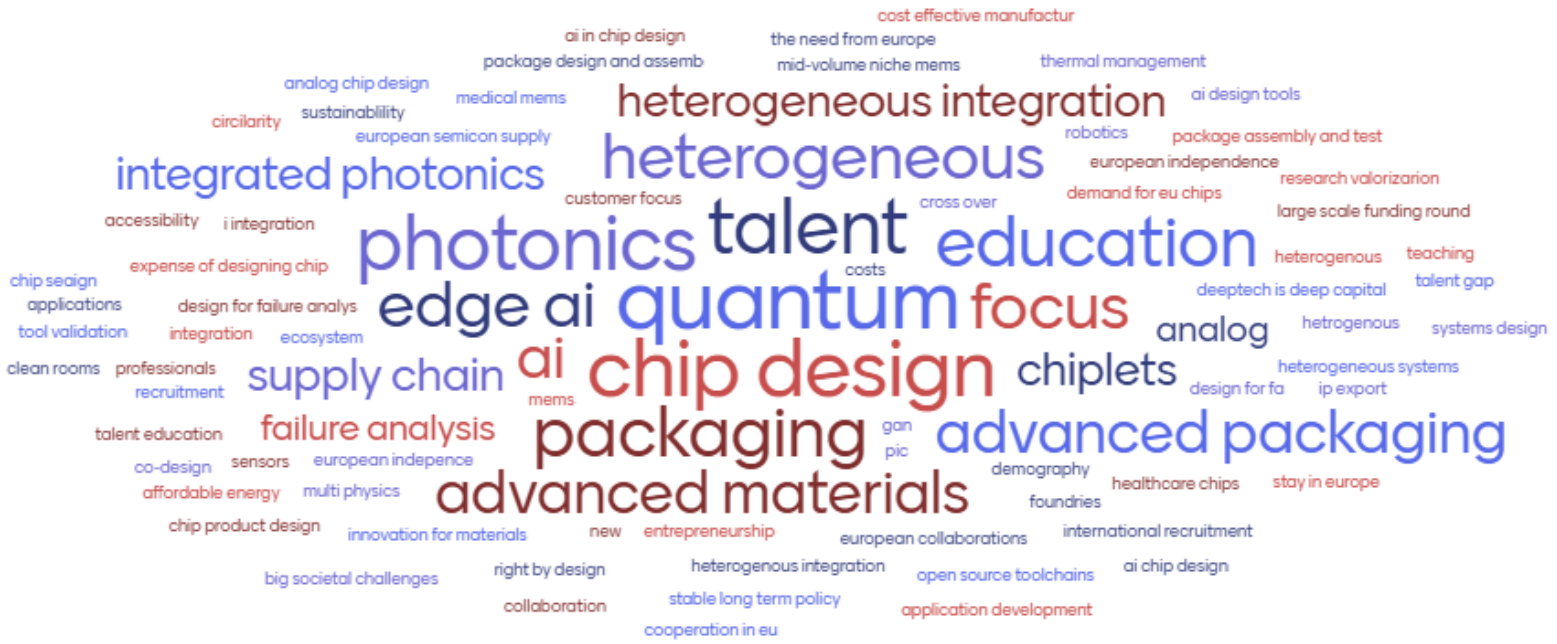
Which broader technological trends or gaps should be prioritized in the review of the Chips Act?



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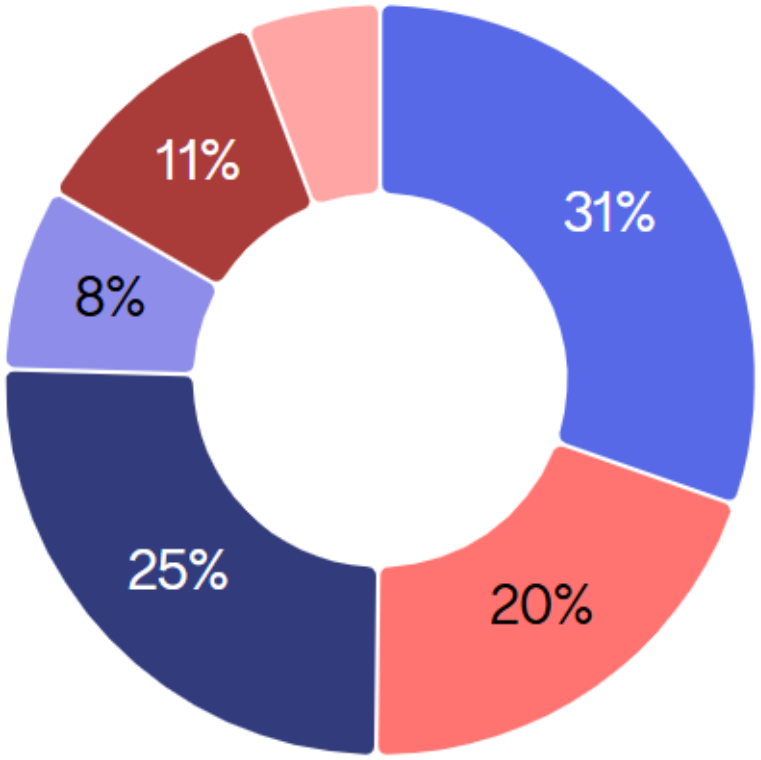
Through international cooperation, what types of action could be taken to strengthen the EU's ecosystem, and in which specific areas?



31%	Collaboration R&D and innovation
20%	Cooperation on supply chain diversification and security of supply
25%	Workforce development and talent exchange
8%	Cooperation on standardisation
11%	Cooperation on energy-efficient manufacturing techniques and recycling programs for semiconductor materials
6%	Other actions

Let’s keep in touch

<u>At upcoming (partner) events & important dates:</u>

- **PIC Summit** – 4-5 November at Evoluon Eindhoven
- **Global Semiconductor Conference Malta** – 10-11 November at Hilton Malta
- **Technical Deep Dive APECS Pilot Line** – 11 November Webinar 10.00-11.00
- **SEMICON Europe** – 18-21 November at Munchen Messe
- Call for Evidence; **Public consultation for EU Chips Act 2.0** – deadline 28 November (via ec.europa.eu)
- **EFECS** European Forum for Electronic Components and Systems – 2-4 December at Hilton Malta
- **Lifeport Semicon Event** – 27 January 2026 at Goffertstadium Nijmegen
- **Innovation Mission to South Korea** – 9-13 February 2026 (registration before 10-Nov via RVO.nl)

→ Stay tuned at **cccnl.nl/events** & follow us on LinkedIn at **ChipNL Competence Centre**

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