German Chips
Competence Centre

Forschungsfabrik
Mikroelektronik
Deutschland

Germany’s Gateway to European Semiconductor Infrastructure

German Chips Competence Centre (G3C) as a Central Hub Connecting the German Semiconductor Ecosystem with the European Design Platform and Pilot Lines

Alexander Stanitzki, Senior Project Manager G3C

German Chips Competence Centre (G3C)

Objectives and Relations

Access and Guidance:
The G3C **acts as an intermediary for** chip design services, infrastructure and tools.

Awareness:
G3C creates a **catalogue of value propositions** and supports cross-border collaboration.

Knowledge:
G3C provides **courses and training on heterointegration** and other focus topics of the German ecosystem.

Network:
G3C cooperates in the **ENCCC network** and with other chips related initiatives.

G3C Project office and
Expert team from 12 institutes

Connects to APECS and more than 15 technology clusters in Germany

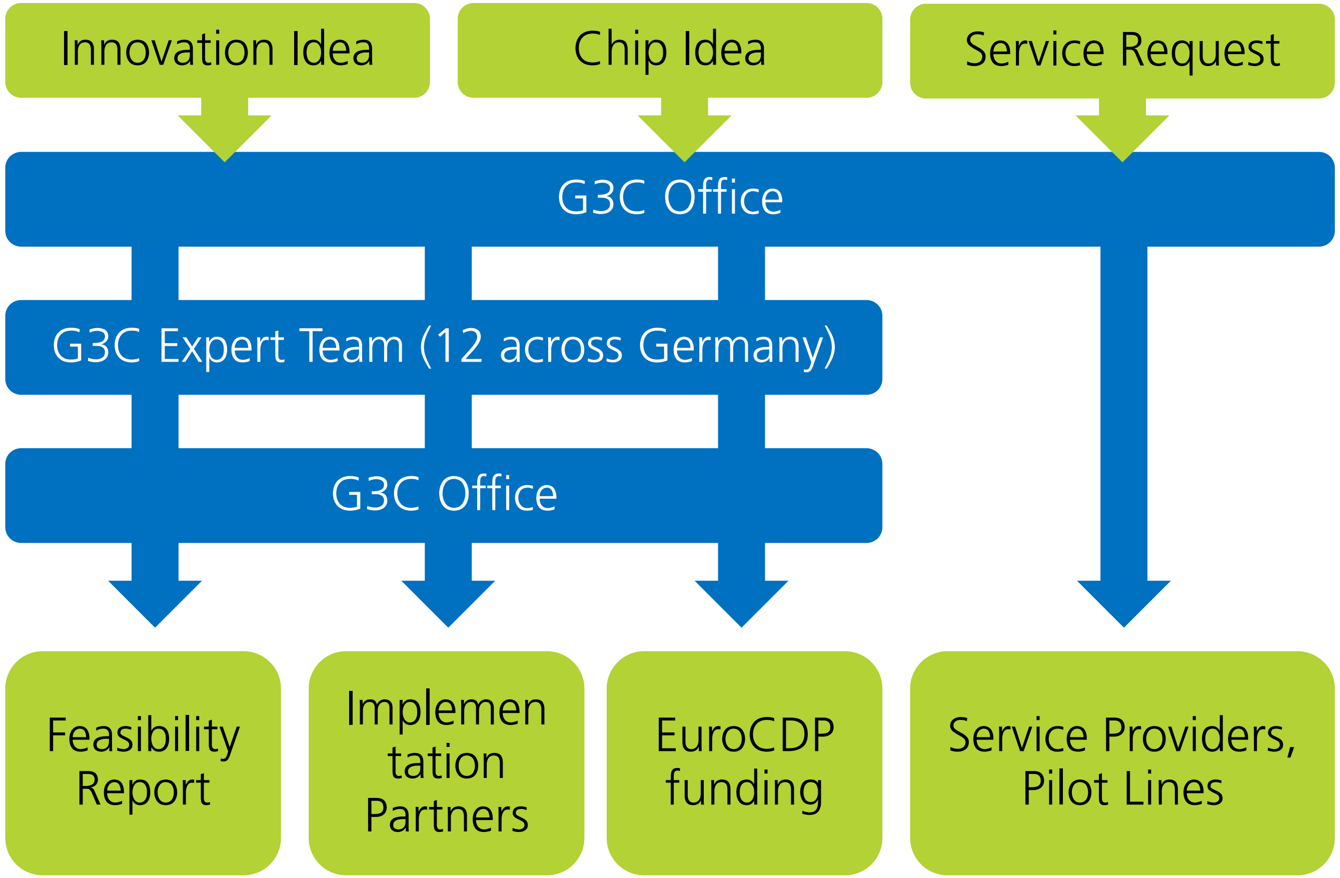
www.german-chips.de

German Chips Competence Centre (G3C)

Main service: Access and Guidance

Access and Guidance:

- The G3C office maintains a list of service provider and implementation partners (pilot line related and other) and **will broker between ideas and implementers.**
- Early-stage ideas are reviewed by an **expert group** to determine technical constraints, cost and time estimation.
- G3C **reports to the client** with suggestions on feasibility, potential partners and funding sources.

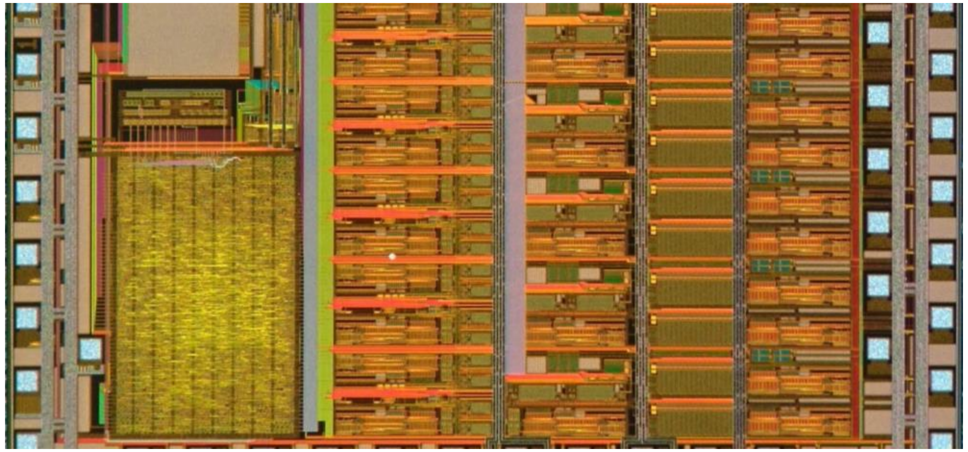


German Chips Competence Centre (G3C)

An example

Transition from prototype to MVP

Startup has an FPGA prototype for a wearable health monitoring device, including an innovative algorithmic twist. They ask for guidance to develop an ASIC.



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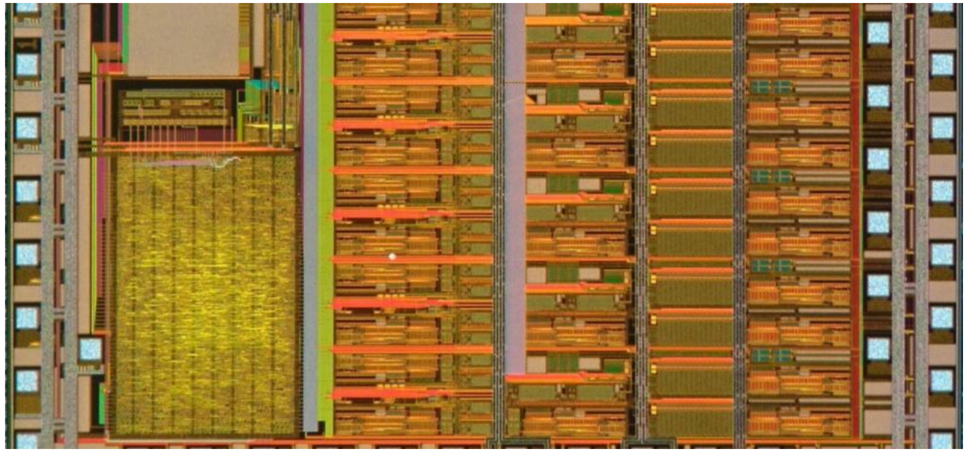

Discussion of USPs, current architecture and time plan with G3C office; exchange of NDA an request form

week 1

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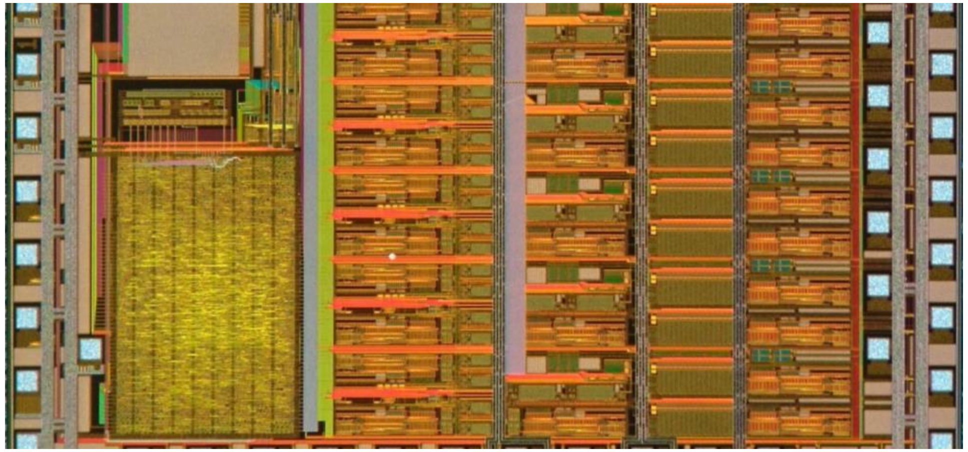

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Technical expert group retrieves missing information

G3C office lists tool access and prototype funding options, contacts EuroCDP

week 2

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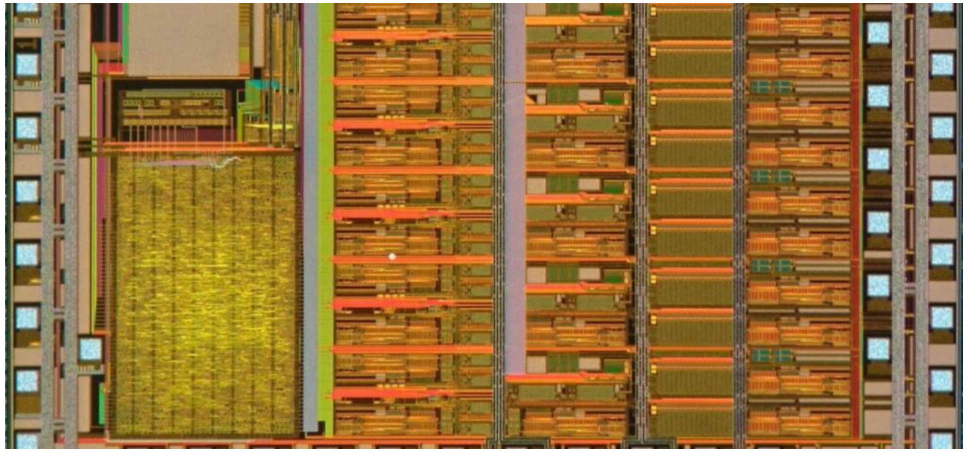

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Discussion of results, ASIC scope definition

week 3

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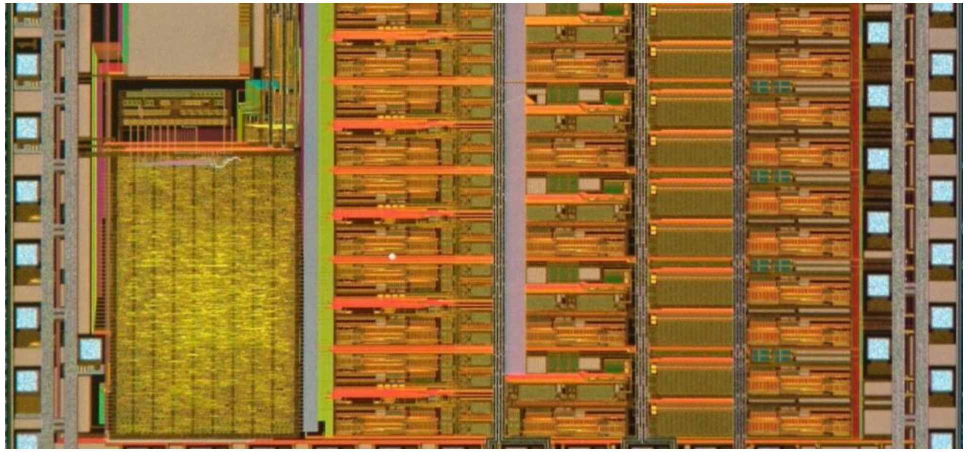

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week 2

Discussion of results, ASIC scope definition

week 3

G3C compiles list of implementation partners

week 4

Thanks for Your Attention

Contact

Alexander Stanitzki
Senior Project Manager G3C

+49-170-2743301
alexander.stanitzki@mikroelektronik.fraunhofer.de

G3C Business Office

c/o Research Fab Microelectronics Germany
Anna-Louisa-Karsch-Str. 2
10178 Berlin (Germany)

www.german-chips.de
info@german-chips.de

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Research Fab Microelectronics Germany (FMD)

A cooperation of 13 Fraunhofer institutes and the Leibniz institutes FBH and IHP

Profile and Specifics

Research Fab Microelectronics Germany (FMD)

13 Fraunhofer and

2 Leibniz institutes

> **5,400*** employees, including > **2,900*** scientists

First patent applications: **191**

Active patent families: **2986**

19,500 m²
cleanroom space

ISO9001 certification

1 MES over 10 institutes

> **2,200 tools/equipment** in **13 cleanrooms**

€ 2.2 bn	Assets/Investment
€ 673 m	Budget/a
€ 272 m	Industry projects

- Applied research with solid foundation in academic research/education and technology transfer as a mission
- Research on heterogeneous systems integration and advanced packaging on EU level for technological sovereignty within the EU Chips Act
- Special commitment to green ICT, quantum and neuromorphic computing, chip design, heterogeneous systems integration and trusted electronics

- Project oriented funding model with small share of basic funding
- Strong link to applications / industry
- Distributed structure as group of institutes
- Young talent development

*Number of employees incl. AISEC and IMWS. Given figures relate to 2023.

Research Fab Microelectronics Germany (FMD)

Cooperation between 13 Fraunhofer and 2 Leibniz institutes

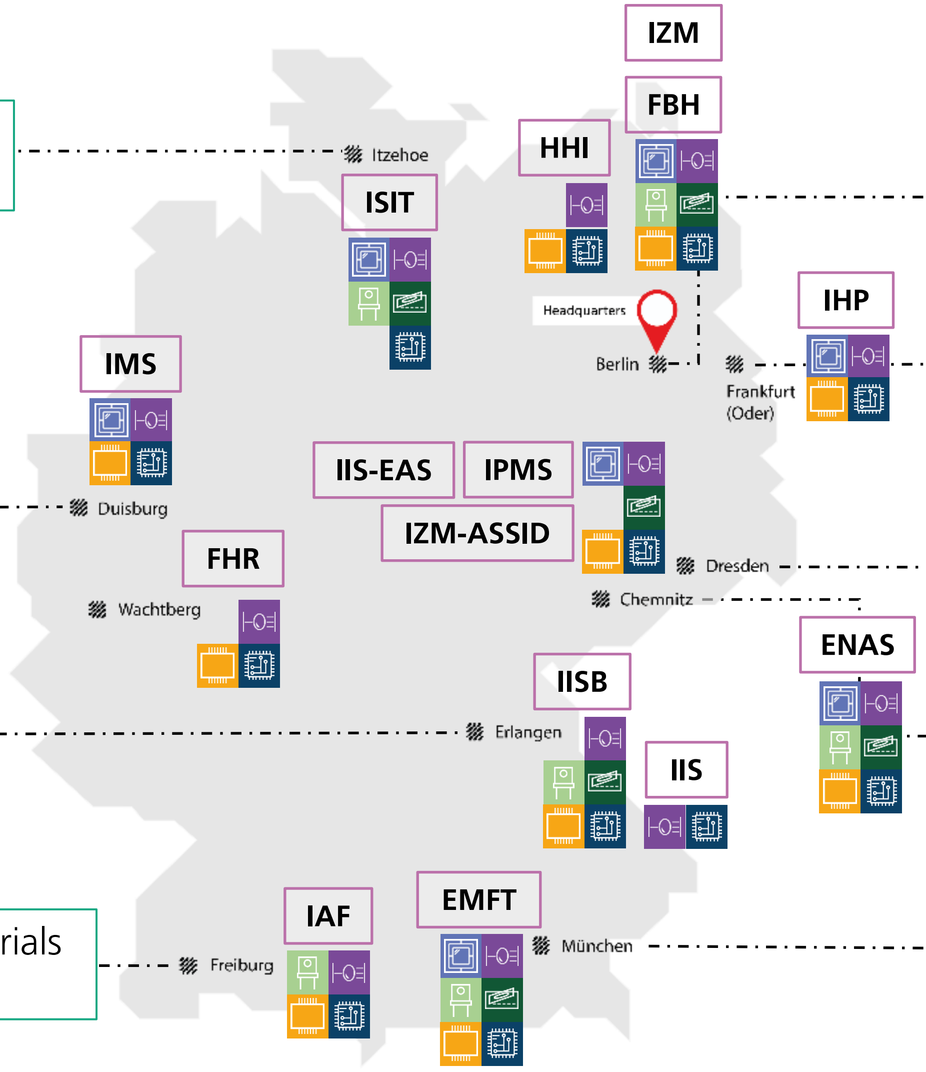
Fraunhofer Institute for

- Applied Solid State Physics **IAF**
- Applied and Integrated Security **AISEC**
- Electronic Nano Systems **ENAS**
- High Frequency Physics and Radar Techniques **FHR**
- Integrated Circuits **IIS**
- Integrated Systems and Device Technology **IISB**
- Microelectronics Circuits and Systems **IMS**
- Microstructure of Materials and Systems **IMWS**
- Electronic Microsystems and Solid State Technologies **EMFT**
- Telecommunications, Heinrich-Hertz-Institut **HHI**
- Photonic Microsystems **IPMS**
- Silicon Technology **ISIT**
- Reliability and Microintegration **IZM**

Leibniz Institutes

- Ferdinand-Braun-Institut gGmbH, Leibniz-Institut fuer Hoechstfrequenztechnik **FBH**
- Leibniz-Institute for High Performance Microelectronics **IHP GmbH**

FMD Cleanrooms and Technology Platforms all over Germany



200 mm MEMS
200 mm GaN-on-Si

200 mm MEMS
200 mm CMOS/Si

200 mm CMOS/Si
150 mm SiC

4“ Compound Materials
200 mm GaN-on-Si

4“ Compound Materials
4“ InP
200 mm Packaging

200 mm (Bi)CMOS

300 mm CMOS/Si
300 mm Packaging
200 mm MEMS

200 mm MEMS

200 mm CMOS/Si
200 mm MEMS

FMD Technology Platforms

- Extended CMOS
- Optoelectronic Systems
- Power Electronics
- MEMS Actuators
- Microwave and Terahertz
- Sensor Systems

Technology Platforms

Research Fab Microelectronics Germany

1 **Sensor Systems**
Sensor design, fabrication, integration, characterization, and testing within systems

2 **Microwave and Terahertz**
Cutting-edge devices and circuits for frequencies up to and including the THz range

3 **MEMS Actuators**
Design and fabrication, as well as characterization, testing and system integration of MEMS actuators

4 **Extended CMOS**
Design, fabrication and system integration of CMOS circuits

5 **Power Electronics**
Design and fabrication of power electronic devices, including integration in modules and systems

6 **Optoelectronic Systems**
Fully integrated optoelectronic systems for image acquisition and processing, and communication up to Tbit/s speed

7 **Chip- und Chiplet-Design**
Design of computer chips in which either a single integrated circuit (chip) is developed or several small, independent chips (chiplets) are integrated into a system in order to optimise performance, efficiency and functionality

8 **Multi Project Technologies (MPT)**
Product prototyping / IP verification / Design libraries / Device characterization / Low volume manufacturing / “Proof of concept”/ Experiments with new circuits / First Silicon verification

APECS

Forschungsfabrik Mikroelektronik Deutschland

Peak Performance in Heterogeneous Integration

Pilot Line for Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems (APECS)

Research Fab Microelectronics Germany (FMD)

Coordinated by

Fraunhofer

Implemented by

Forschungsfabrik Mikroelektronik Deutschland

Pilot Line Project Partners

- Fraunhofer MIKROELEKTRONIK
- Leibniz Ferdinand Braun Institut (FBH)
- ihp
- TU Graz
- VTT
- imec
- cea leti
- FORTH FOUNDATION FOR RESEARCH AND TECHNOLOGY - HELLAS
- cnm CENTRO NACIONAL DE MICROELECTRÓNICA / CSIC CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS
- INL INTERNATIONAL IBERIAN NANOTECHNOLOGY LABORATORY

Co-funded by

- Chips JU
- Co-funded by the European Union
- With funding from the: Federal Ministry of Research, Technology and Space
- Freistaat SACHSEN
- BERLIN
- Bayerische Staatsregierung
- SH Schleswig-Holstein Landesregierung
- Baden-Württemberg
- Die Landesregierung Nordrhein-Westfalen
- LAND BRANDENBURG
- SACHSEN-ANHALT
- Ministry of Economic Affairs and Employment of Finland
- ANI AGÊNCIA NACIONAL DE INOVAÇÃO
- RÉPUBLIQUE FRANÇAISE Liberté Égalité Fraternité
- Flanders State of the Art
- HELLENIC REPUBLIC MINISTRY OF DEVELOPMENT
- Federal Ministry Republic of Austria Climate Action, Environment, Energy, Mobility, Innovation and Technology
- MINISTERIO PARA LA TRANSFORMACIÓN DIGITAL Y DE LA FUNCIÓN PÚBLICA
- BUSINESS FINLAND
- CCDR NORTE
- anr agence nationale de la recherche
- FFG Promoting Innovation.

APECS is co-funded by the Chips Joint Undertaking and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain, through the Chips for Europe Initiative.

APECS Work Flow

Connecting design, technology and testing

Design Flows

System Design

Interface Processing: Chiplet integration

Hetero-integration into (quasi-)monolithic integration (QMI)

Chiplet Integration platform (2.5D and 3D)

Analysis & Metrology

Character., Test & Reliability

Demos & Application Solutions

- STCO Design for 2.5D / 3D
- STCO Design for QMI
- Foundational Chiplets

STCO = System Technology Co-Optimization
QMI = Quasi-monolithic integration

Front End Integration:

- RF Integration
- Photonic Integration
- QMI-Systems

HF = High frequency
QMI = Quasi-monolithic integration

Back End Integration:

- Advanced Packaging
- Functional Integration
- Functional Interposer

- Characterization
- Reliability
- Test

Access via One-Stop-Shop

Thanks for Your Attention

Contact

Felix Mohn
Manager Business Development

felix.mohn@mikroelektronik.fraunhofer.de

APECS Business Office

c/o Research Fab Microelectronics Germany
Anna-Louisa-Karsch-Str. 2
10178 Berlin (Germany)

www.apecs.eu ✉ info@apecs.eu

APECS

Forschungsfabrik
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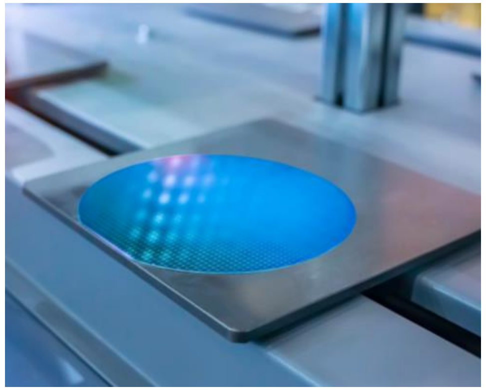
Peak Performance in Heterogeneous Integration

Pilot Line for Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems (APECS)

Anna Lena Schall-Giesecke, Head of Technology, Fraunhofer IMS
IMS-PL: Alexander Litke

Your host today

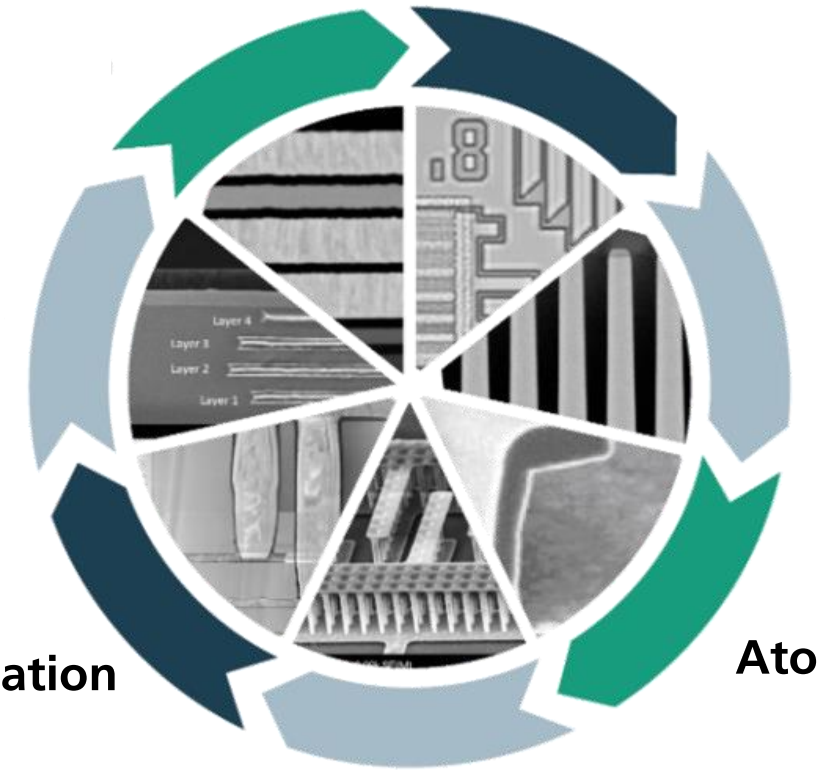
Fraunhofer IMS



- **Cleanroom infrastructure:** 1,900 m² ISO 4; 9001-certified fabrication
- **Scalable production:** From R&D prototyping up to pre-series manufacturing
- **Open integration platform:** Support for novel materials (2D, electro-optics, bio) and application-specific components (microoptics, microfluidics)
- **Heterogeneous integration:** Chiplet-capable; proven post-CMOS integration expertise of microelectronics, MEMS and PIC
- **Flexible design rules:** Application-specific solutions enabled by adaptable design rules

Your host today

Fraunhofer IMS



250 nm DUV lithography

Deep reactive ion etching

Atomic layer deposition

Sacrificial etching

2.5D and 3D integration

Metrology

Low temperature deposition

APECS Pilot Line

Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems

DURATION
11/2024–6/2029

FUNDING
730 million euros in total

FUNDED BY
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COORDINATION
Fraunhofer-Gesellschaft

IMPLEMENTATION
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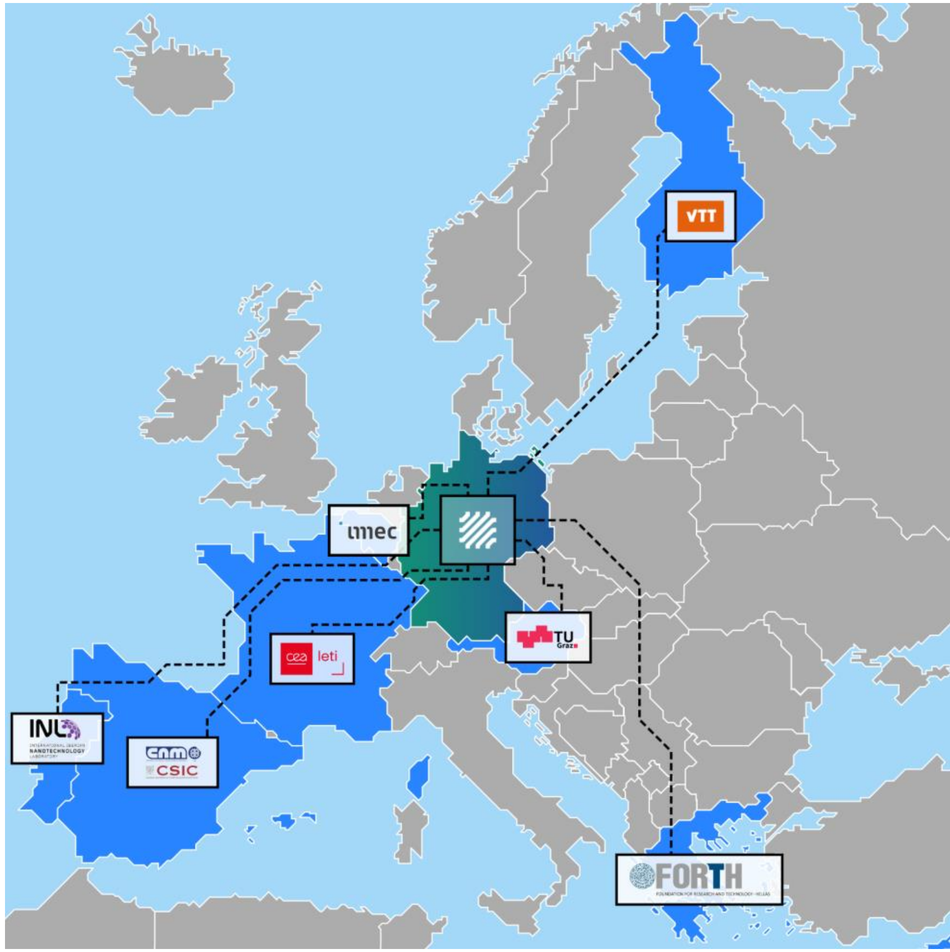

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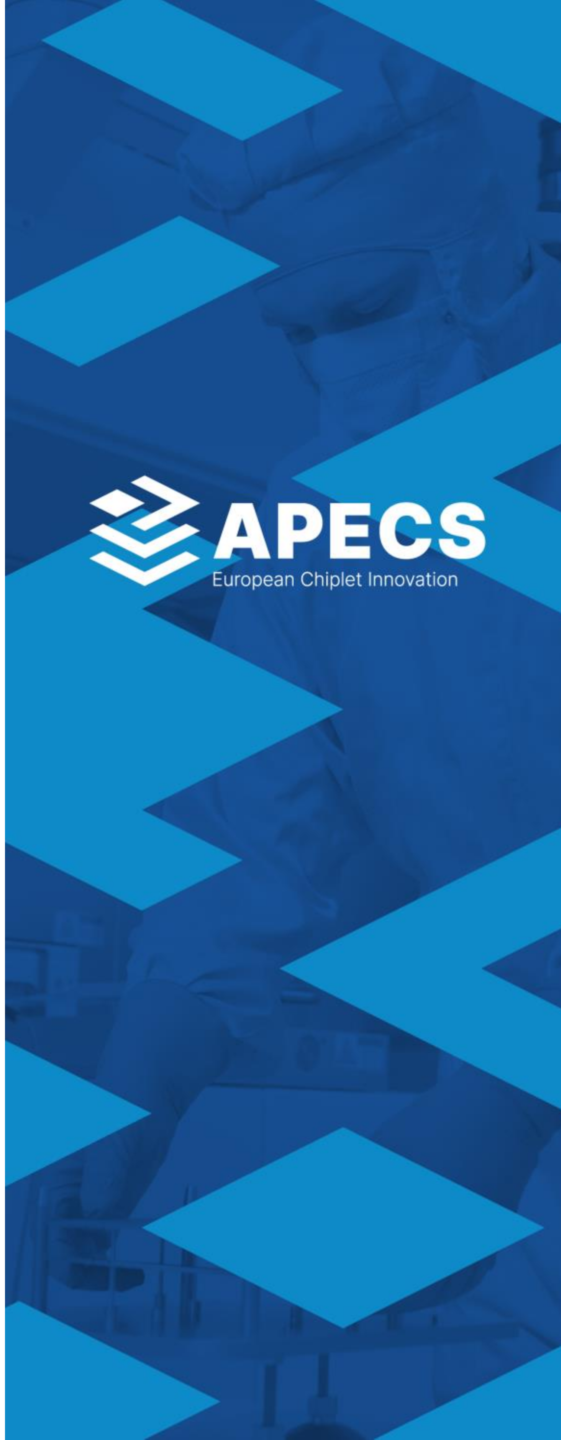
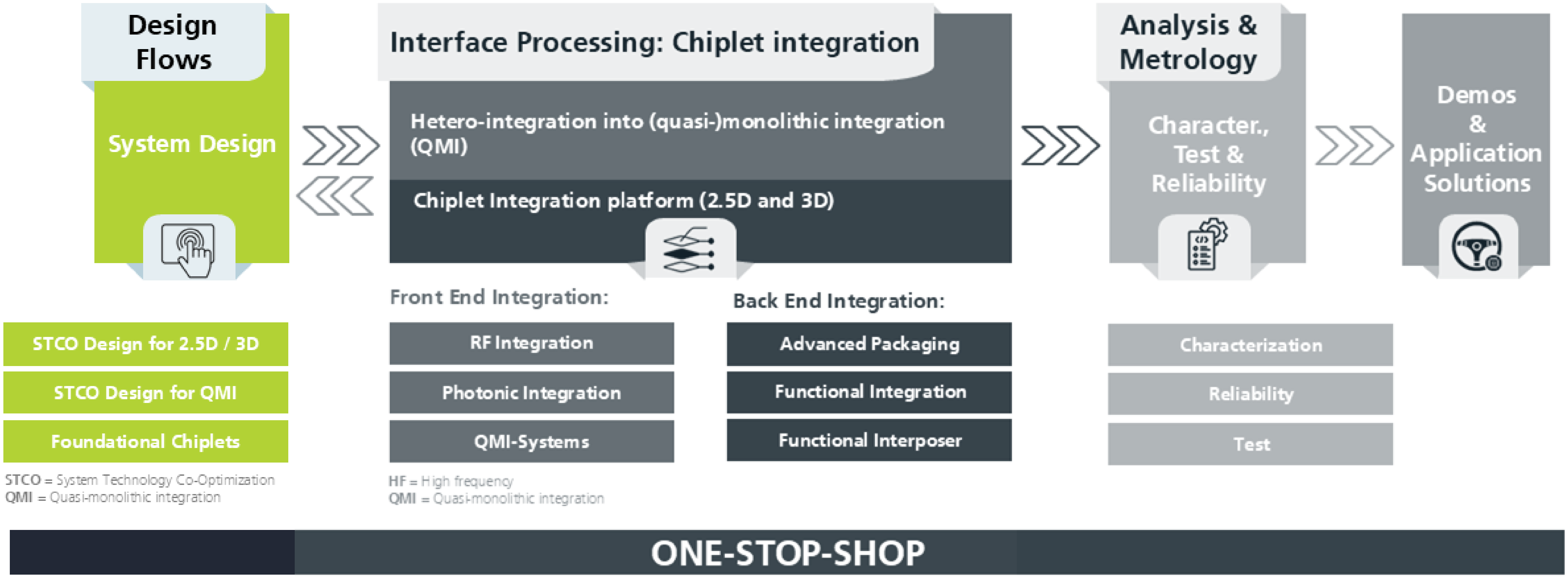
APECS Pilot Line

Main Topics

- **The holistic system design** as access to an efficient and robust design environment for fully integrated systems as well as the fundamental ability to create system designs in the new technologies.
- **Development** and provision of **technological process chains for component and chiplet integration using advanced packaging technologies** to implement a chiplet-based system concept
- **Characterization, Test & Reliability (CTR)**, in which new concepts for quality assurance, safety and yield improvement are developed and provided.



APECS Pilot Line



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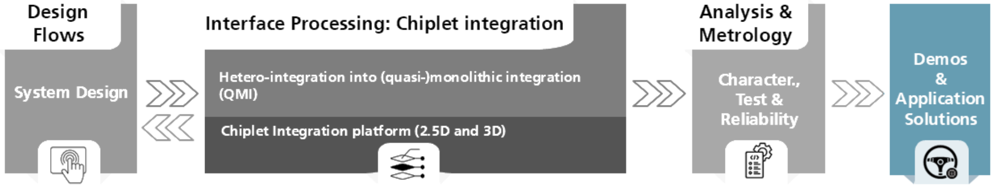
- Characterization
- Reliability
- Test

ONE-STOP-SHOP

Demonstrator

Multi-Material Sensors



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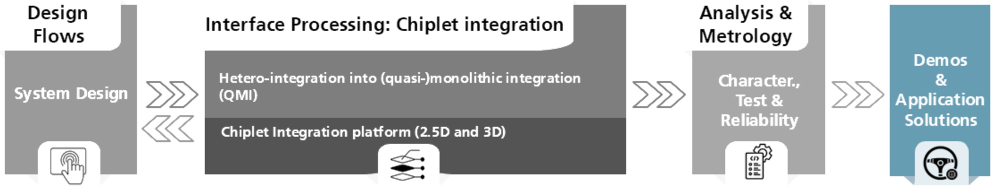
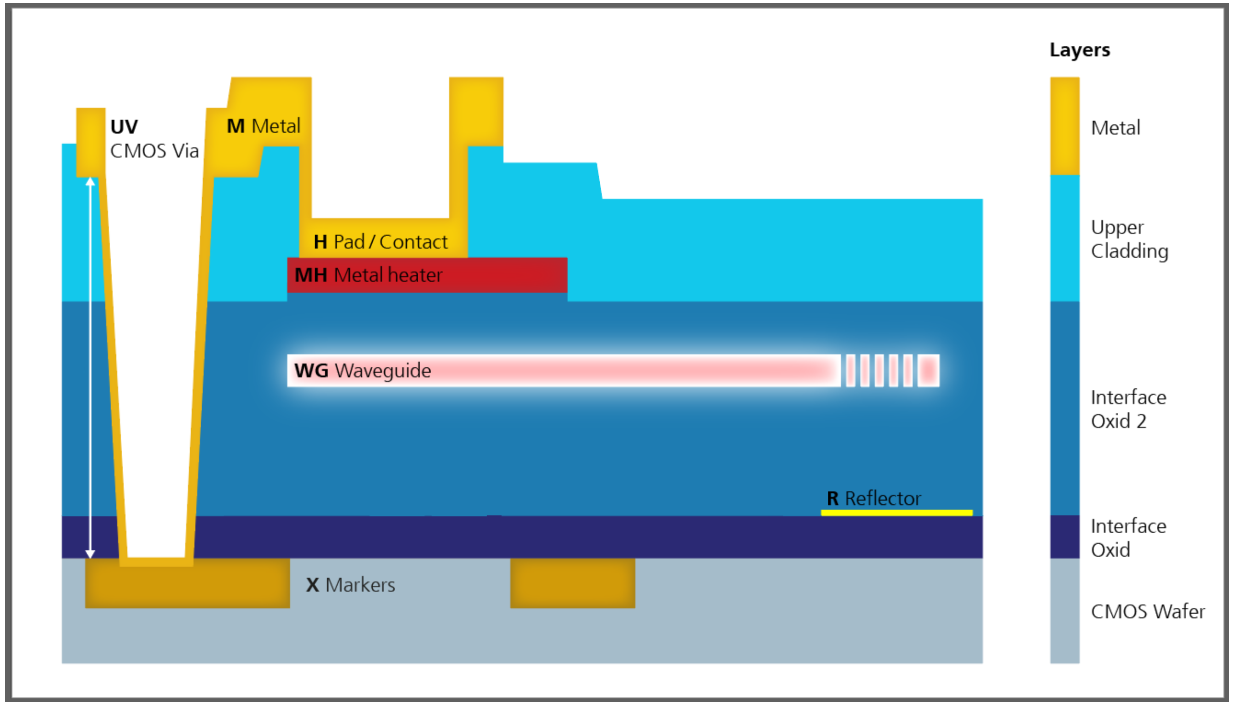
Demos & Application Solutions

- 4 different chiplets:
  1. Acoustic (IPMS)
  2. HEMT GaN (ISIT)
  3. MEMS mirror (IPMS)
  4. **Post-CMOS Photonic (IMS)**
- Si-Interposer with individual redistribuition layers (ENAS)

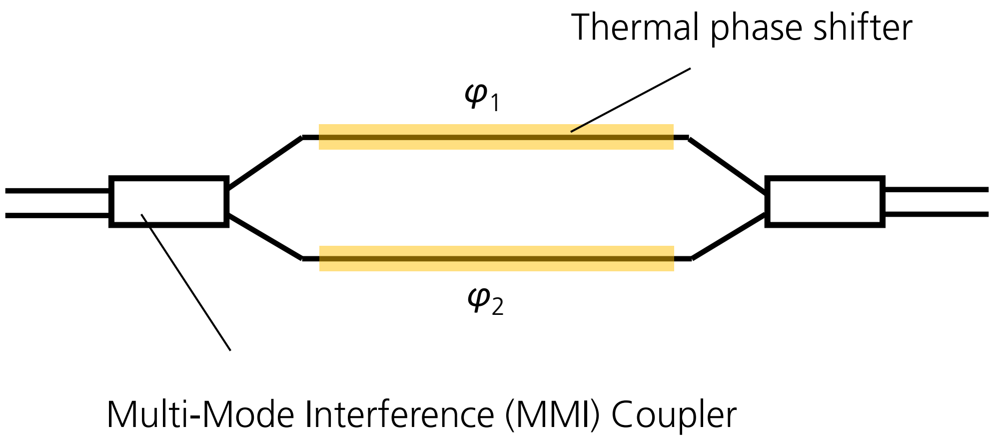
Demonstrator

Post-CMOS Photonic Integrated Circuits at IMS



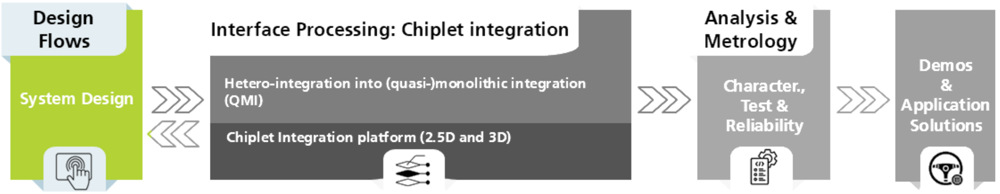


Mach-Zehnder Interferometer (MZI)

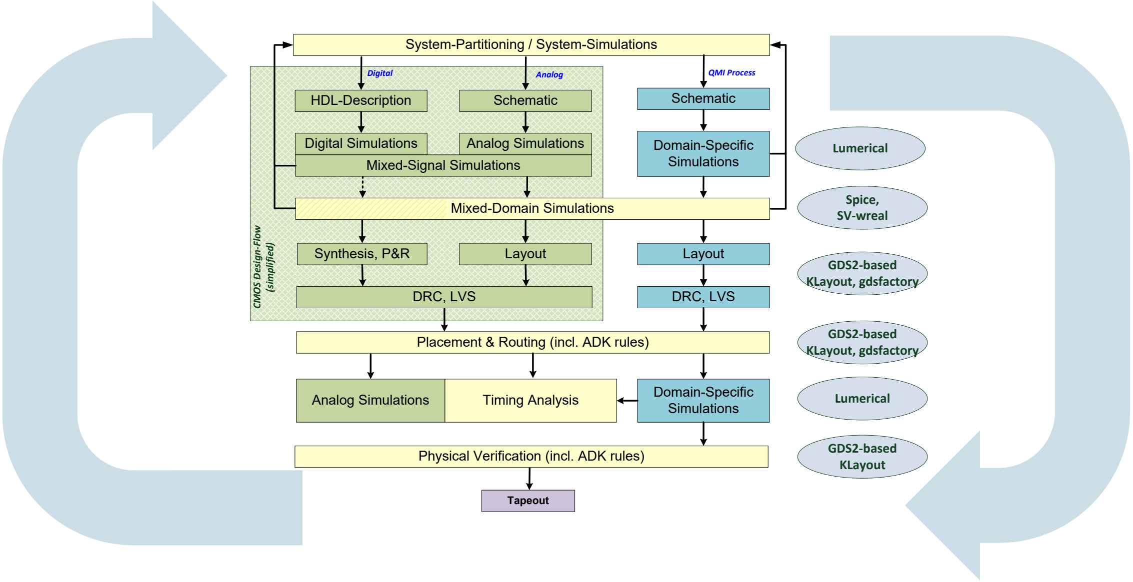


Design flows

System Technology Co-Optimization (STCO)



IMS STCO-Flow



Main Results:

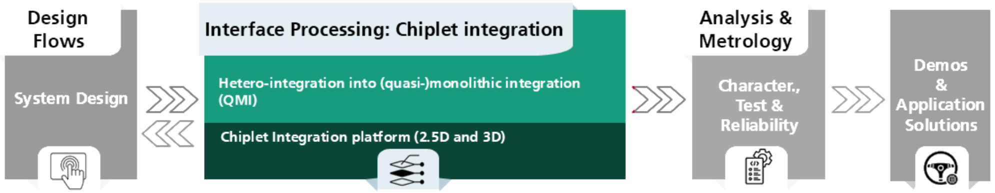
Component libary

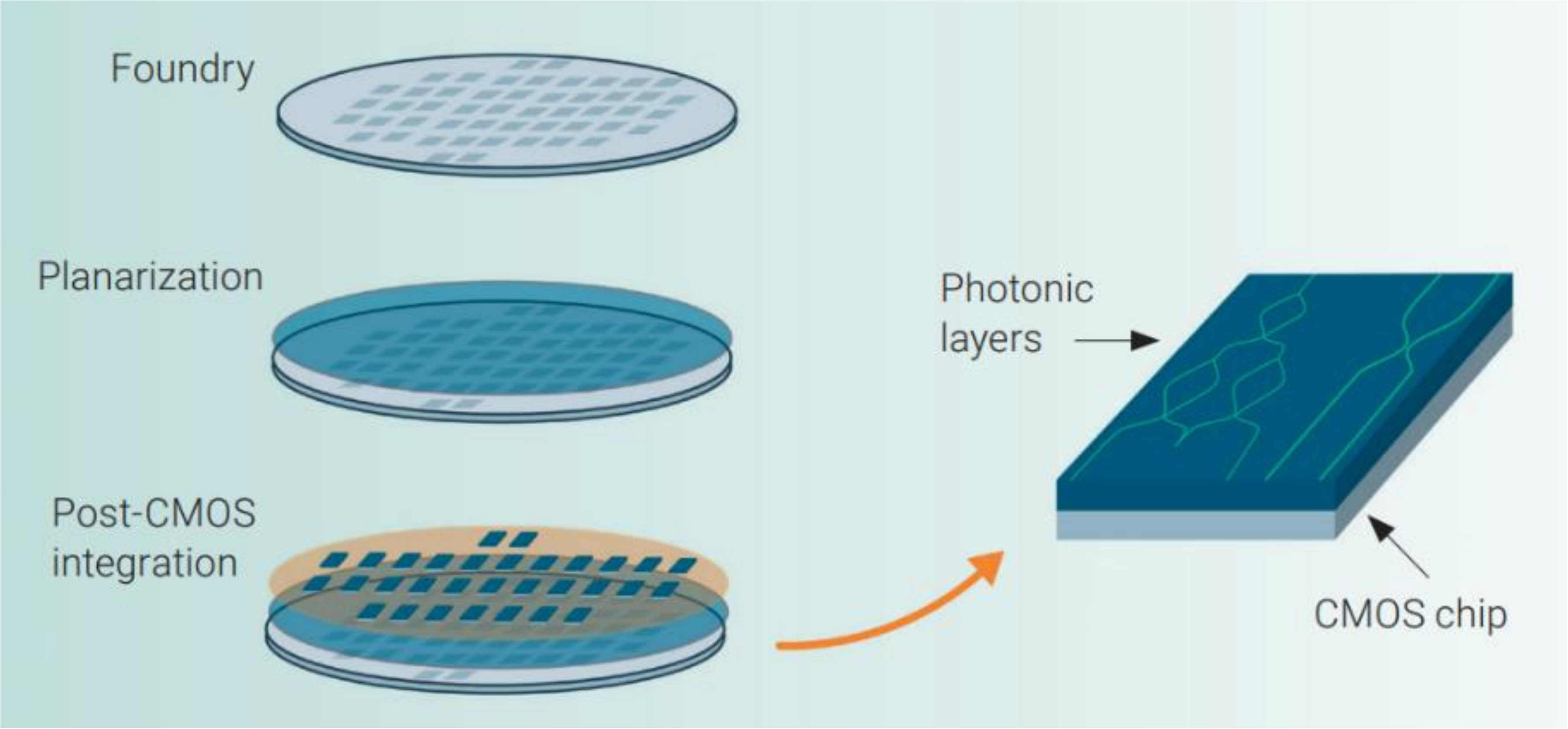
PDK & ADK for different technologies:

- Post-CMOS photonics
- Post-CMOS IR detectors
- Design-Flow for Multi-Process Hetero Integration

Versatile 200 mm post-CMOS Photonics

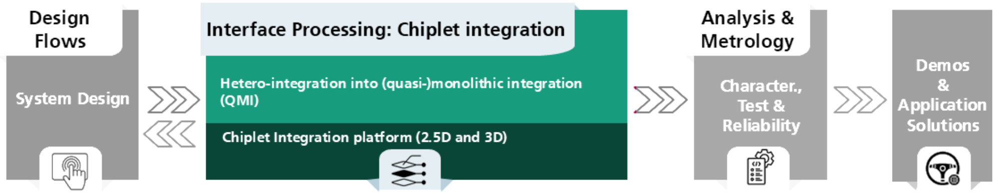
Post CMOS Integration Platform





Versatile 200 mm post-CMOS Photonics

Flexible dielectric waveguide platform: wavelengths



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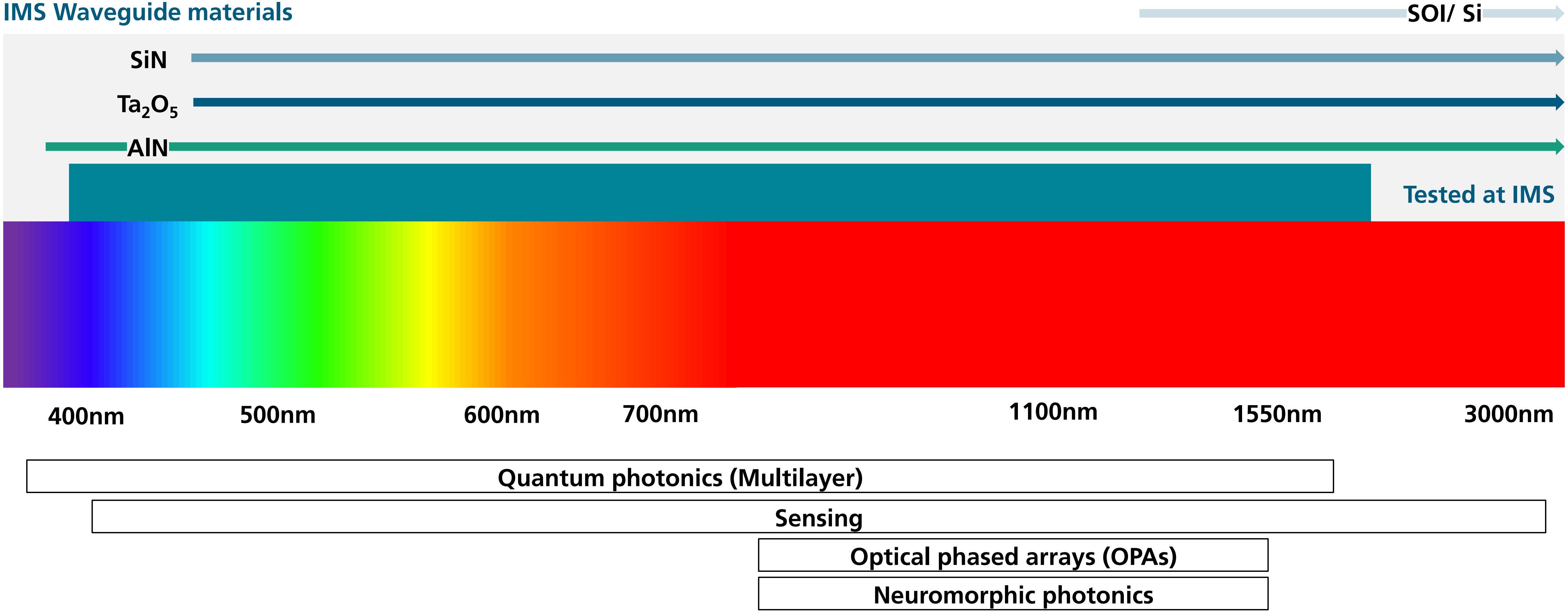
Demos & Application Solutions

IMS Waveguide materials



SOI/ Si

SiN

Ta_2O_5

AlN

Tested at IMS

400nm
500nm
600nm
700nm
1100nm
1550nm
3000nm

Quantum photonics (Multilayer)

Sensing

Optical phased arrays (OPAs)

Neuromorphic photonics

APECS

Versatile 200 mm post-CMOS Photonic Plattform

Material Overview

Material	Optical loss	Properties and Applications	Deposition Techniques
Silicon nitride	Low loss	Post-CMOS and Waveguides only	▪ Low pressure chemical vapour deposition - LPCVD ▪ Plasma enhanced CVD - PECVD ▪ Sputtering
Aluminum nitride	Low loss	Highly transparent up to UV Post-CMOS	Sputtering
Tantalum pentoxide	Ultra low-loss	Thin waveguide Post-CMOS	Atomic Layer Deposition (ALD)

Versatile 200 mm post-CMOS Photonics

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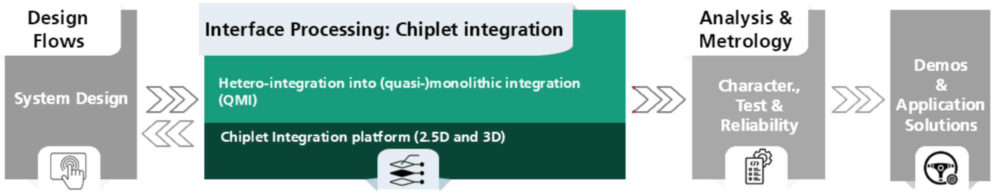
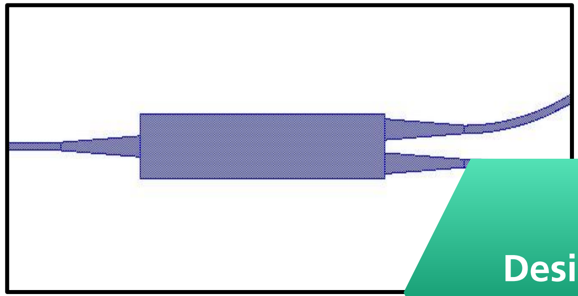
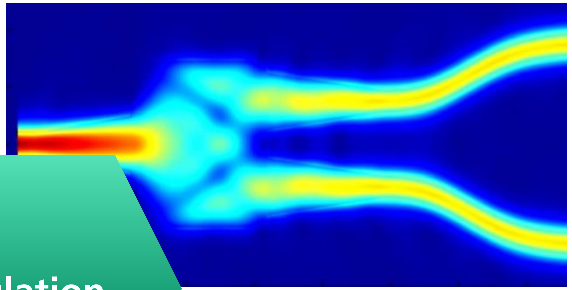






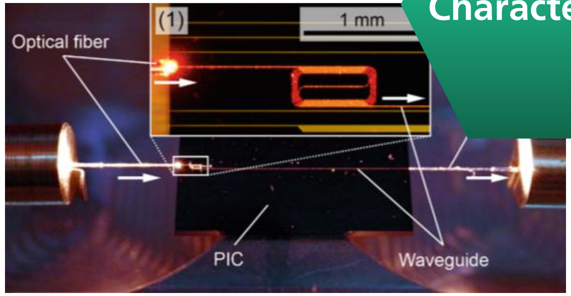
Design / Layout

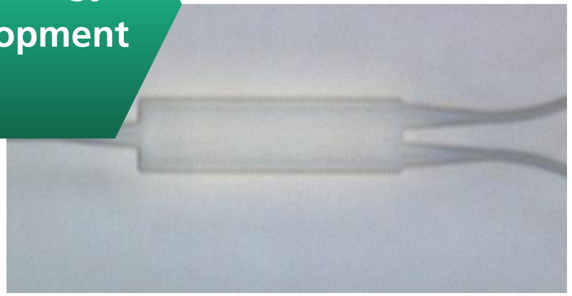
Simulation

Electronics & Photonics

Characterization

Technology Development

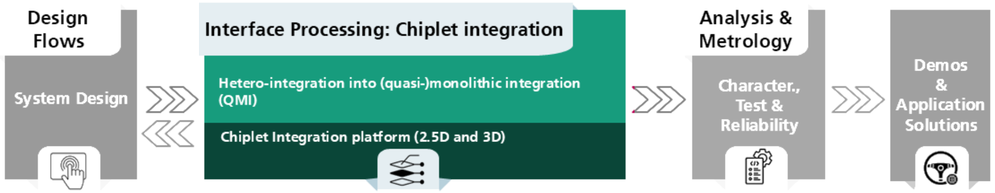




We are an experienced upscaling partner for start-ups/ scale-up!

Post-CMOS Photonics platform

IMS Integration platform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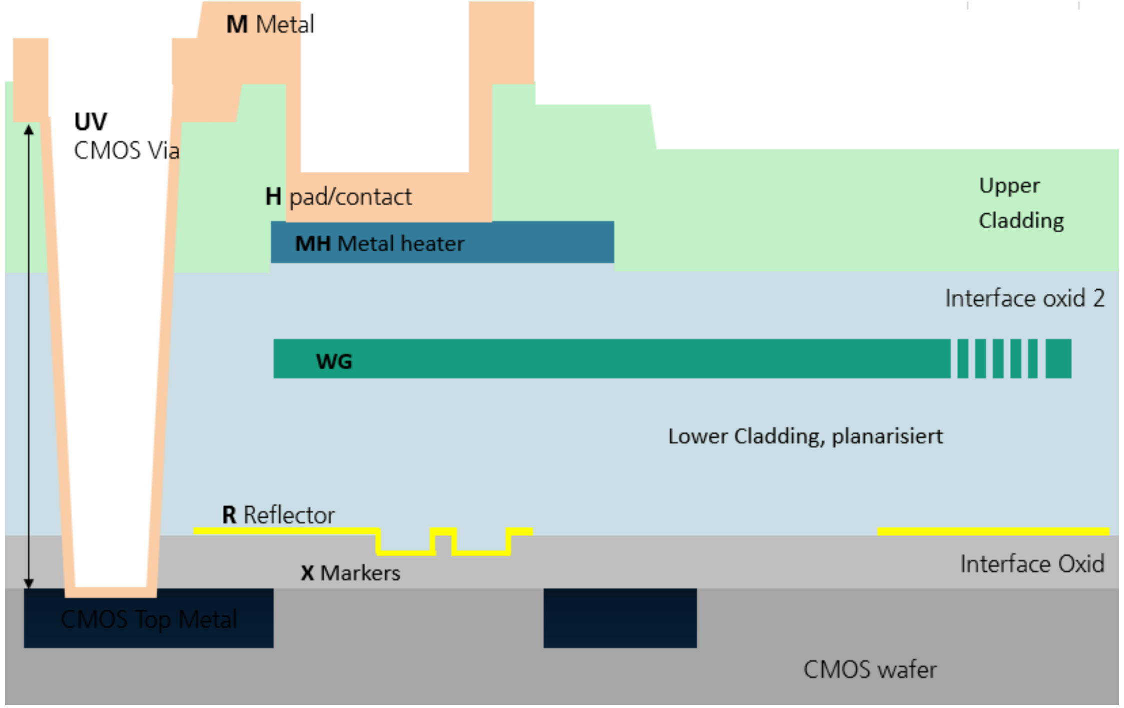
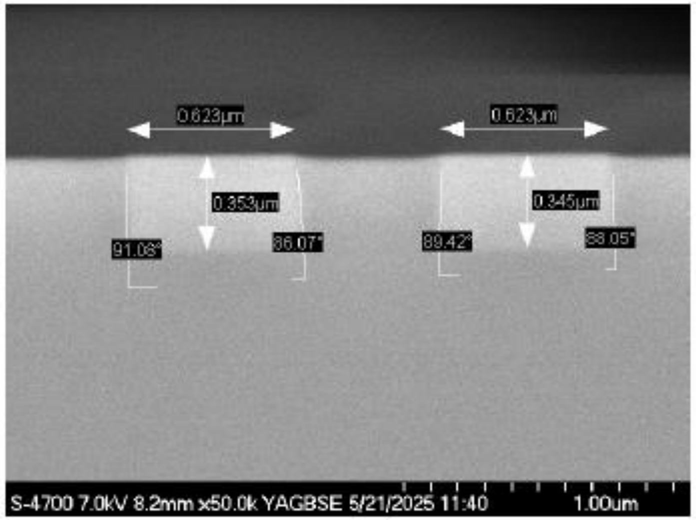
Exemplarily Post-CMOS Photonics stack

Cross section



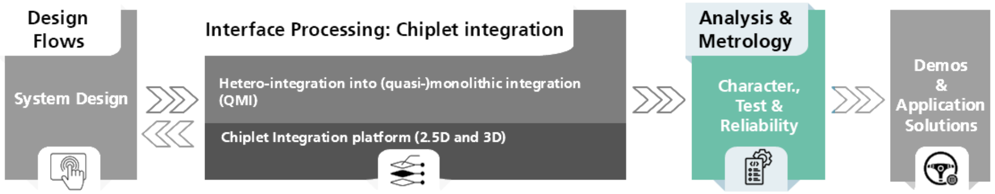
Material integration after chemical mechanical polishing (CMP)

SEM cross section image



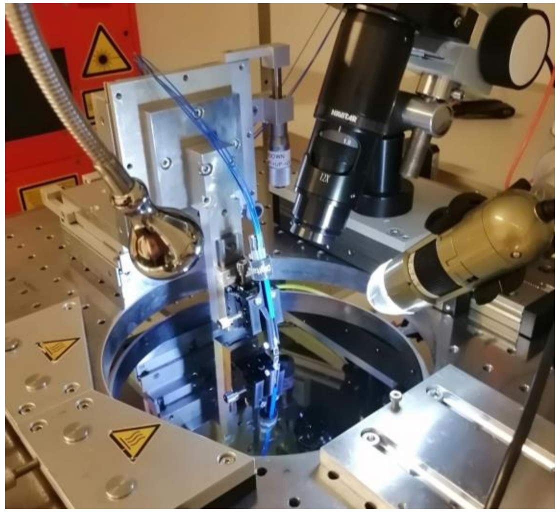
Characterization & Test

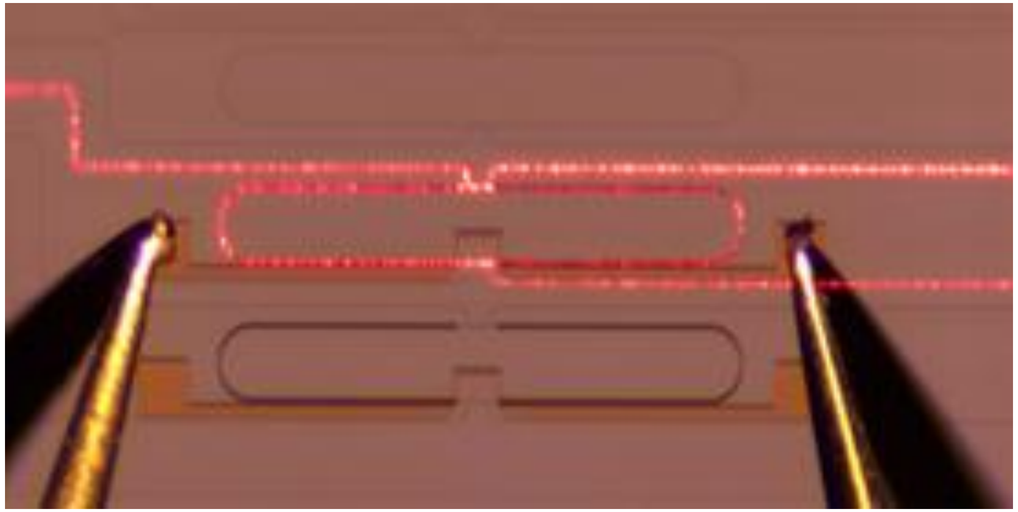
Services at IMS



1. Fully automated setup (casette to casette) → to be installed
2. Single photon quantum setup → to be installed
3. Nolinear photonics setup → under construction

Semi automated setup (wafer-scale): electro-optical characterization for wavelengths 400 nm – 2 µm (available)



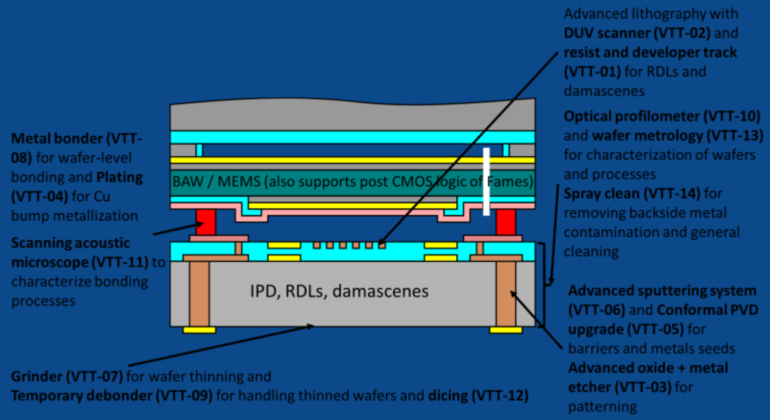


Joint Technology Development by VTT & Fraunhofer IZM, ENAS, IMS, IPMS

6G and optical MEMS technologies

Jointly Developed Technology: Key Features

- IPD and RF components on silicon and glass substrates
- Heterogenous 3D integration: **ALD for TSV**
- Wafer Level and LTCC Packaging of RF and optical MEMS
- Procurement, installation and set-up of the pilot line equipment at VTT



Advanced lithography with **DUV scanner (VTT-02)** and **resist and developer track (VTT-01)** for RDLs and damascenes

Optical profilometer (VTT-10) and **wafer metrology (VTT-13)** for characterization of wafers and processes

Spray clean (VTT-14) for removing backside metal contamination and general cleaning

Metal bonder (VTT-08) for wafer-level bonding and **Plating (VTT-04)** for Cu bump metallization

Scanning acoustic microscope (VTT-11) to characterize bonding processes

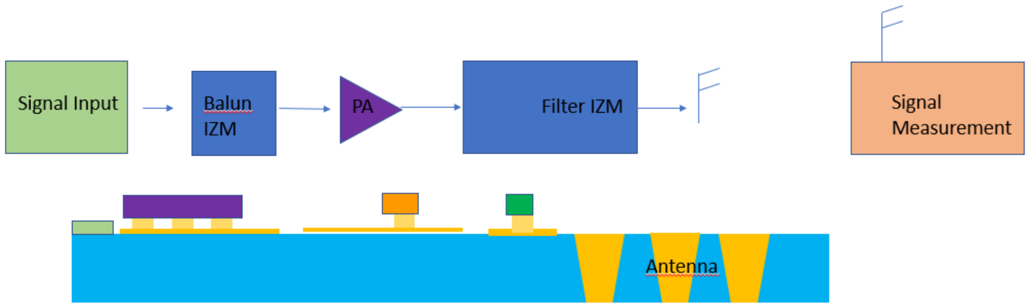
Advanced sputtering system (VTT-06) and **Conformal PVD upgrade (VTT-05)** for barriers and metals seeds

Advanced oxide + metal etcher (VTT-03) for patterning

Grinder (VTT-07) for wafer thinning and
Temporary debonder (VTT-09) for handling thinned wafers and **dicing (VTT-12)**

Demonstrator/Application Areas/Services for industry:

- Glass Interposers, silicon Interposer, equipped with IPD for a wide range of application (e.g. Medical, automotive, industry, photonics)
- Demonstrator showing the capability of all the technologies brought to the project by the different partners on one interposer platform



Coordinated by

Fraunhofer

Implemented by

Forschungsfabrik Mikroelektronik Deutschland

Pilot Line Project Partners

Fraunhofer MIKROELEKTRONIK

Leibniz Ferdinand Braun Institut FBH

ihp

TU Graz

VTT

imec

cea leti

FORTH FOUNDATION FOR RESEARCH AND TECHNOLOGY - HELLAS

CNM CENTRO NACIONAL DE MICROELECTRÓNICA CSIC CONSEJO SUPERIOR DE INVESTIGACIONES CIENTÍFICAS

INL INTERNATIONAL IBERIAN NANOTECHNOLOGY LABORATORY

Co-funded by

Chips JU

Co-funded by the European Union

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Federal Ministry of Research, Technology and Space

Freistaat SACHSEN

BERLIN

Bayerische Staatsregierung

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LAND BRANDENBURG

SACHSEN-ANHALT

APECS is co-funded by the Chips Joint Undertaking and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain, through the Chips for Europe Initiative.

Ministry of Economic Affairs and Employment of Finland

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Federal Ministry Republic of Austria Climate Action, Environment, Energy, Mobility, Innovation and Technology

MINISTERIO PARA LA TRANSFORMACIÓN DIGITAL Y DE LA FUNCIÓN PÚBLICA

BUSINESS FINLAND

CCDR NORTE

anr agence nationale de la recherche AU SERVICE DE LA SCIENCE

FFG Promoting Innovation.

APECS

European Chiplet Innovation

Please feel free to discuss your request with our experts: **experts@apecs.eu**

apecs.eu

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Fraunhofer
IMS

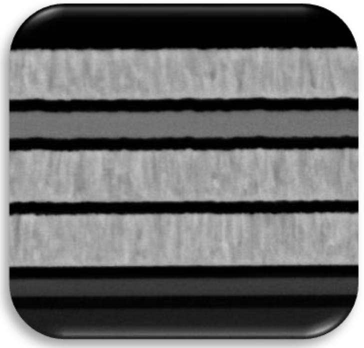
Examples and how to collaborate

Dr. Dorothee Deschmann – Head of Business Unit Silicon Solutions

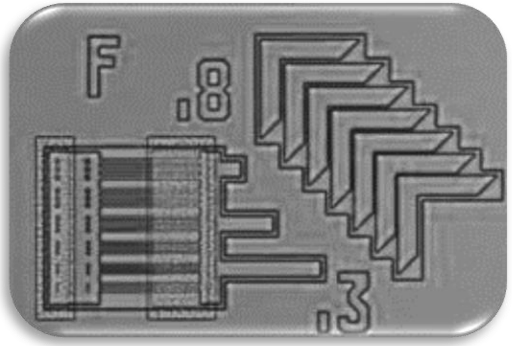
Fraunhofer IMS Technology Services develops with you from R&D to the final product – your partner for high-quality, customized solutions in sensors and ALD as well as expertise in all technology process issues.

Competences

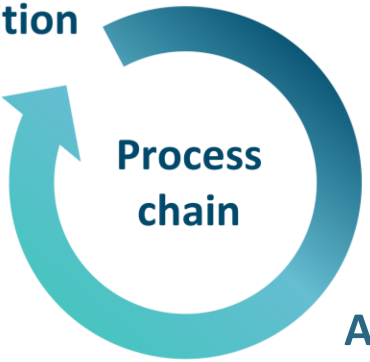
Highest quality standards on industrial level



a-Si, SiGe, Nitride, DLC



0.35 µm



Lithography

Deposition

Process chain

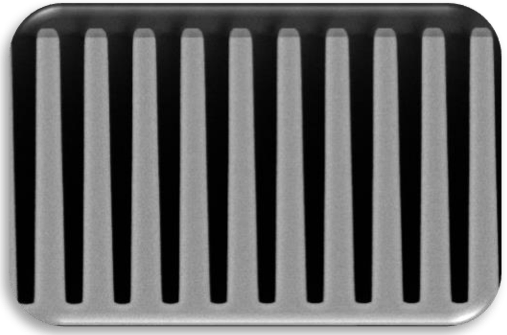
Deep reactive ion etching (DRIE)

Metrology

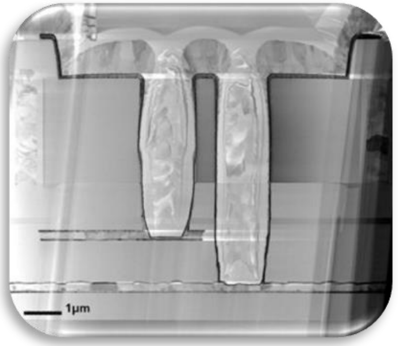
Atomic layer deposition (ALD)

3D integration

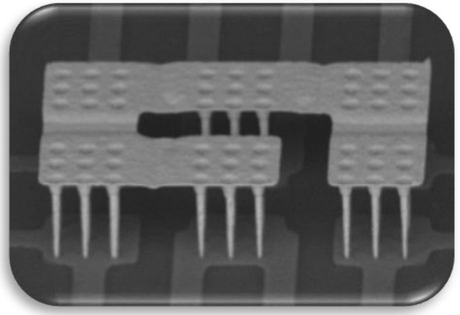
Etching



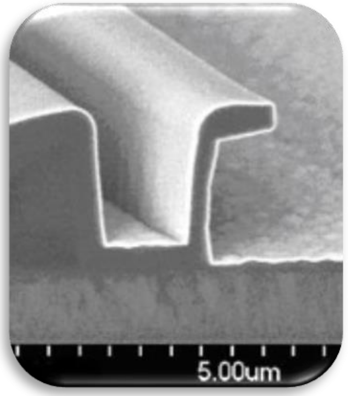
DRIE



µVias



Sacrificial Etching

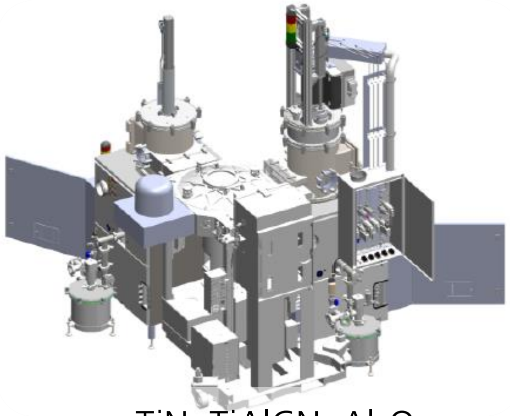


ALD

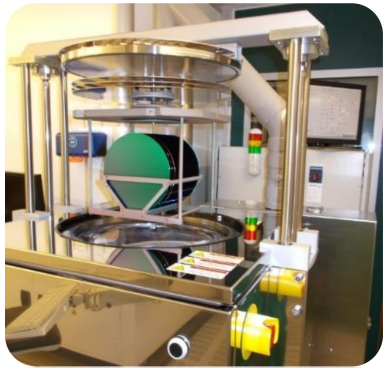
Atomic Layer Deposition

Competence Center within the FMD

- Precise surface coating at **atomic level**
- We offer **outstanding knowledge in precursor chemistry**
- **Precursor screening / Process benchmarking** with new and established precursors in our R&D tool
- Process development of **new materials** like LiPON, Y_2O_3, 2D MoS_2, and more
- Even **special substrates like polymers** can be coated with ALD materials in our **low-temperature processes**



TiN, TiAlCN, Al_2O_3, Ta_2O_5, ZnO, SnO_2, AZO, Ru



Ru, Ta_2O_5, Al_2O_3

SiO_2, TiN, Cu

Al_2O_3, Ta_2O_5, ZnO,TiO_2, HfO_2, Ru, AZO, MoS_2, WS_2

ALD support for every step: from precursor- and process development to pilot production

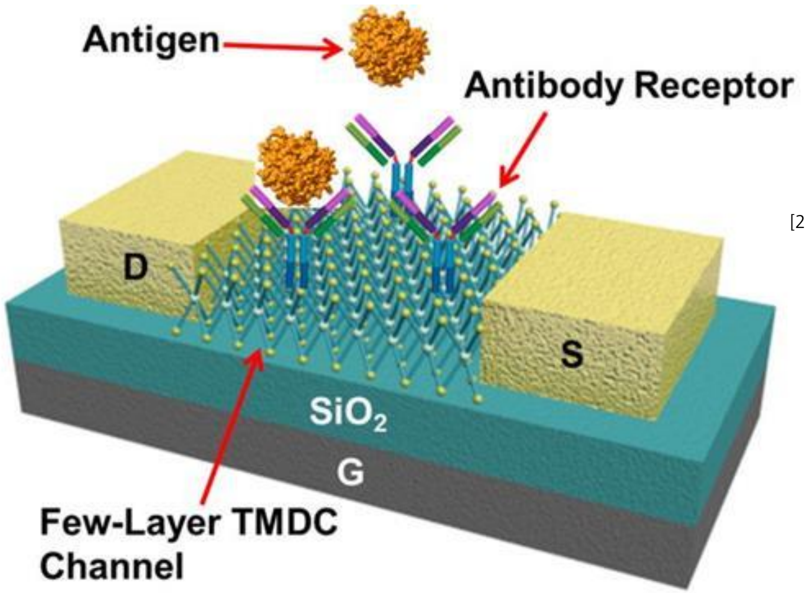
Atomic Layer Deposition

ALD as sensing layer

Benefits of 2D (TMDC) materials

- High sensitivity
- Strong reaction to surface changes
- Low Limit-of-Detection (LOD)
- Fast measurement

Challenges: scalable integration
→ ALD on 200mm wafers instead of exfoliate



[2]

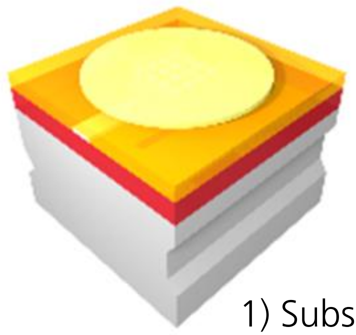
Illustration of a Bio-FET

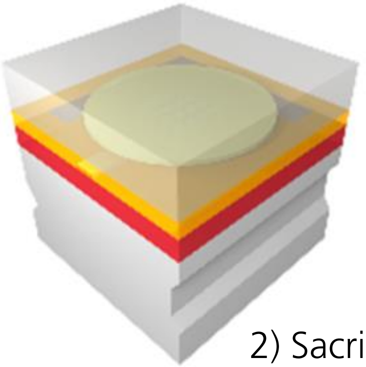
[2]: https://pubs.aip.org/avs/jvb/article/33/6/06FG01/102775/Fabrication-and-comparison-of-MoS2-and-WSe2-field

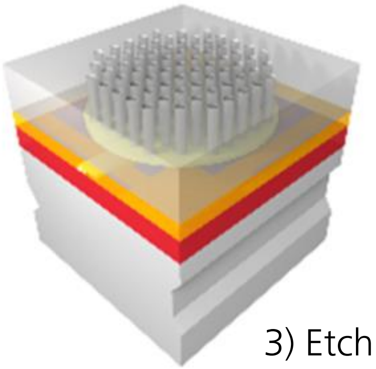
3D Structures

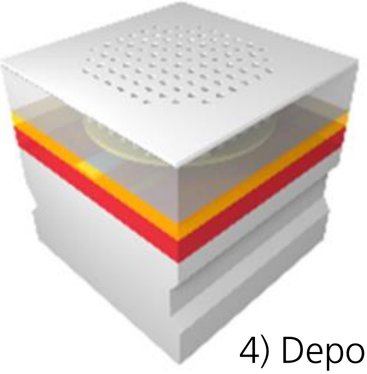
Sacrificial Layer Etching

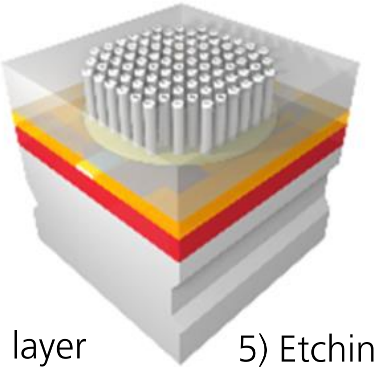
- Patented sacrificial etch technology enabled by ALD

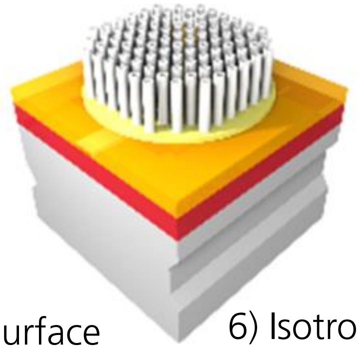

1) Substrate

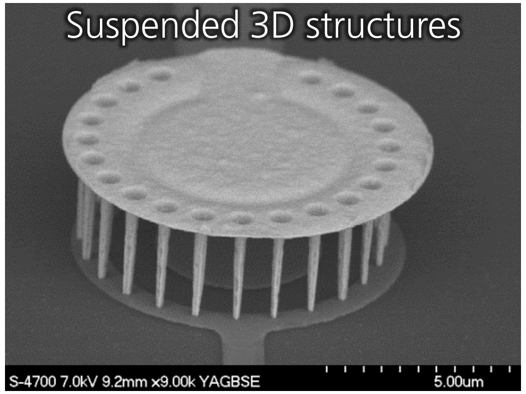

2) Sacrificial layer

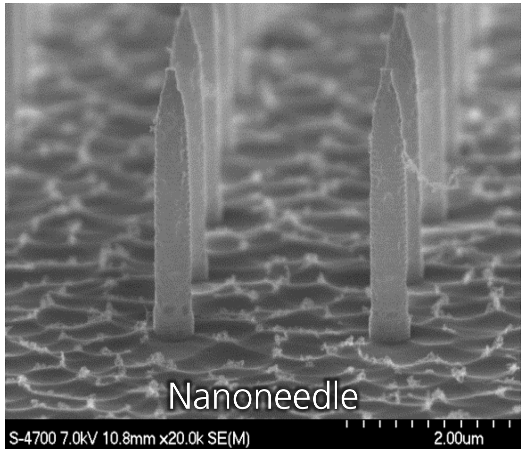

3) Etching holes


4) Deposition of ALD layer


5) Etching the ALD surface

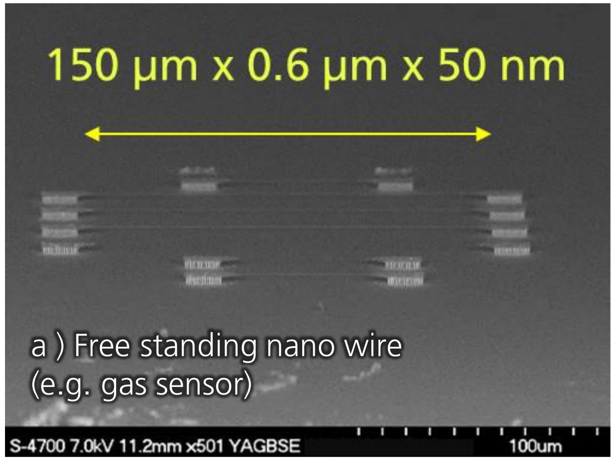

6) Isotropic etching sacrificial layer


Suspended 3D structures

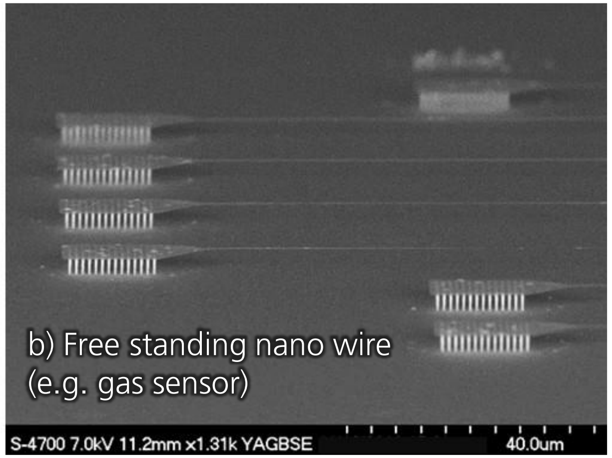

Nanoneedle

3D Structures

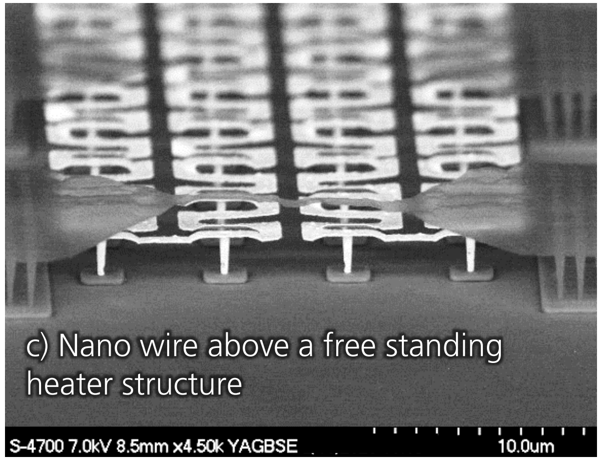
Examples for functional ALD Layers and Structures on 8″ Wafers



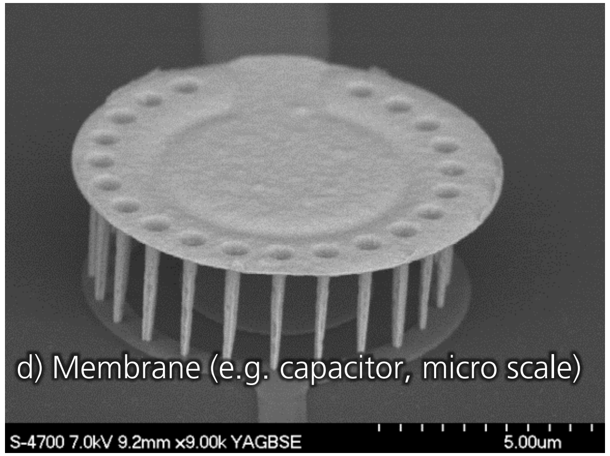
a) Free standing nano wire
(e.g. gas sensor)



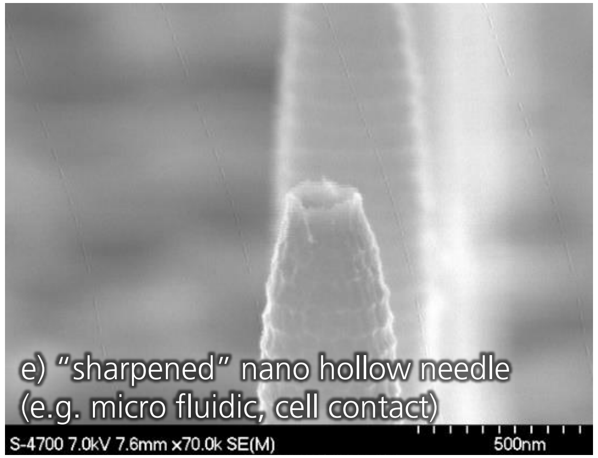
b) Free standing nano wire
(e.g. gas sensor)



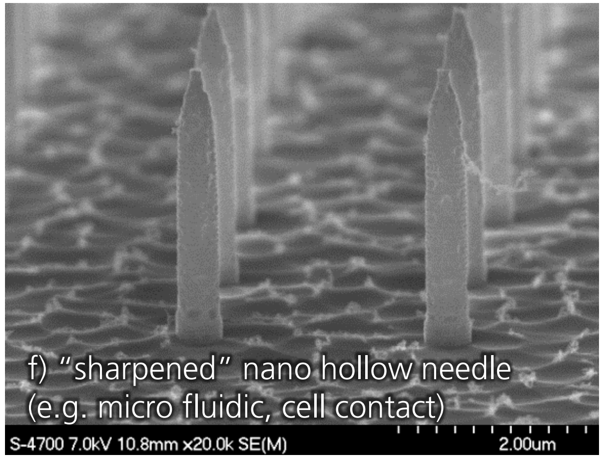
c) Nano wire above a free standing
heater structure



d) Membrane (e.g. capacitor, micro scale)



e) “sharpened” nano hollow needle
(e.g. micro fluidic, cell contact)

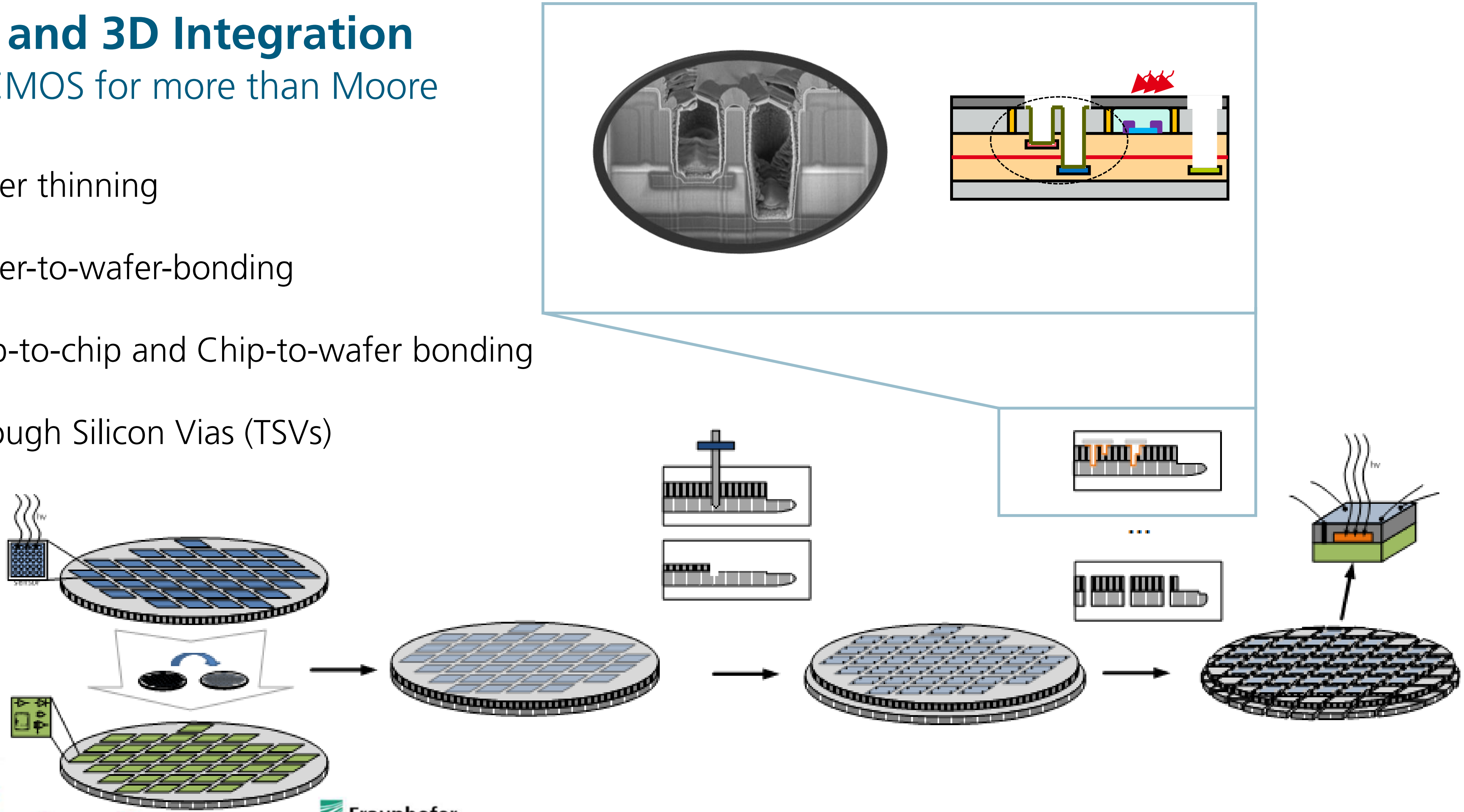


f) “sharpened” nano hollow needle
(e.g. micro fluidic, cell contact)

2.5D and 3D Integration

Post-CMOS for more than Moore

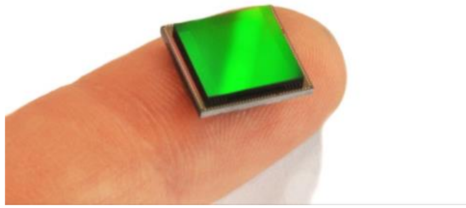
- Wafer thinning
- Wafer-to-wafer-bonding
- Chip-to-chip and Chip-to-wafer bonding
- Through Silicon Vias (TSVs)

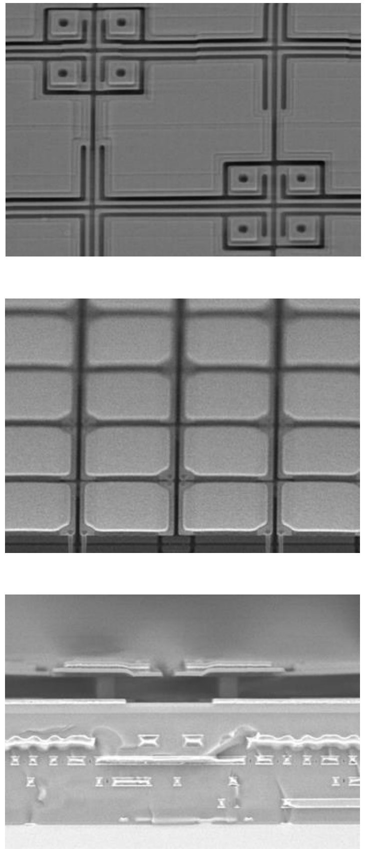


2.5D and 3D Integration

Microbolometer and CPSAD µVias

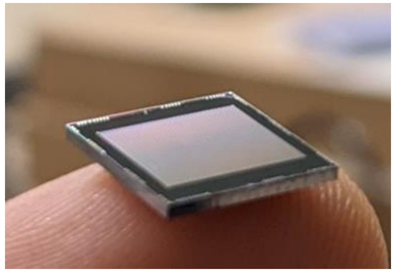
LWIR Imager / Microbolometer

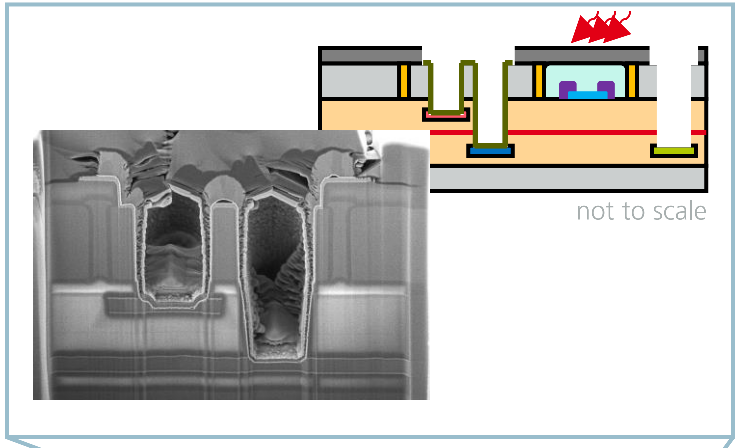




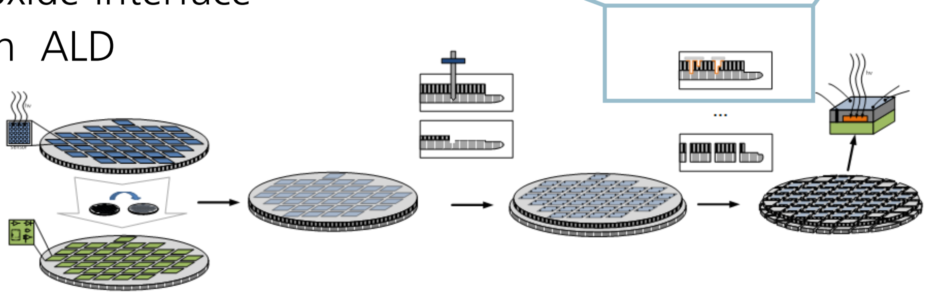
- Bolometer process with 17 µm pixel pitch
- First and only microbolometer process throughout Germany
- Patented sacrificial etch technology
  enabled by ALD

CSPAD detector for LiDAR





- Optical Sensor wafer
- CMOS read-out wafer
- Wafer-to-wafer-bonding with oxide-oxide-interface
- “µVias” with ALD



Post-CMOS Pressure Sensor for Medical Devices

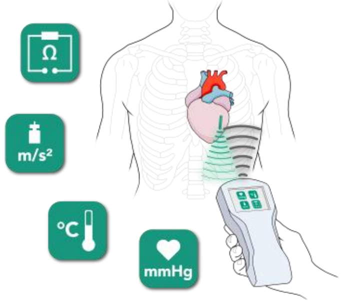
Key pressure sensors developed @ Fraunhofer IMS

2004

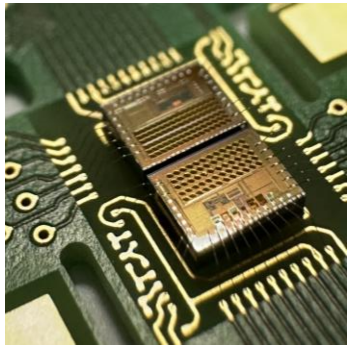
Brain pressure

Eye pressure

Blood pressure



Heart pressure



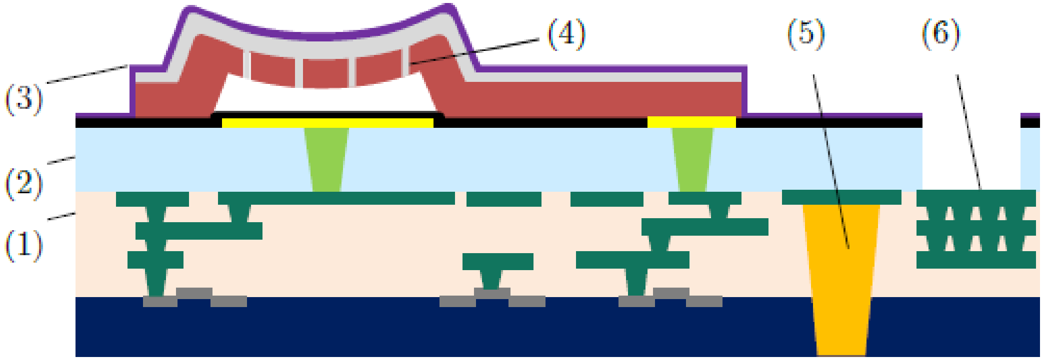
And more

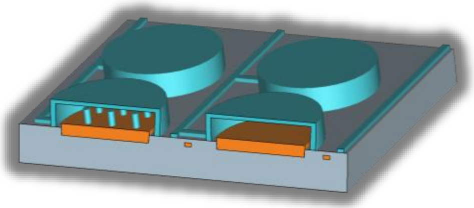
today

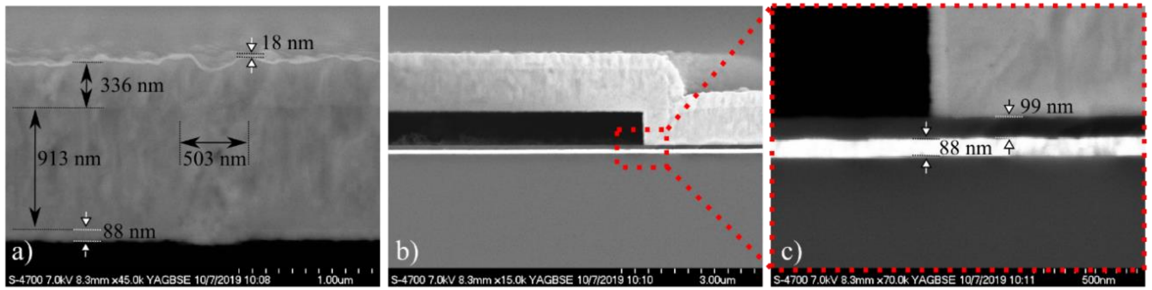
Post-CMOS Pressure Sensor for Medical Devices

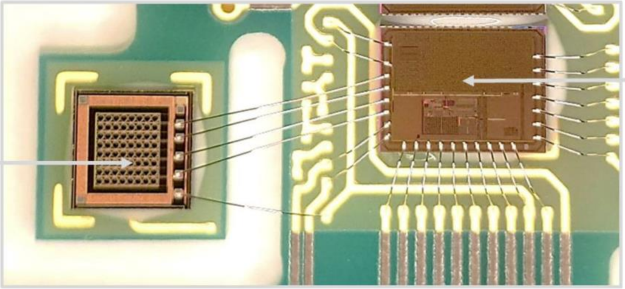
Actual Generation: Used as an implantable shunt sensor

- Monolithic integration onto any CMOS technology
- Capacitive pressure sensing cells on top of flat CMOS passivation
- Drift free
- Long-term stable
- Pressure range tunable by design









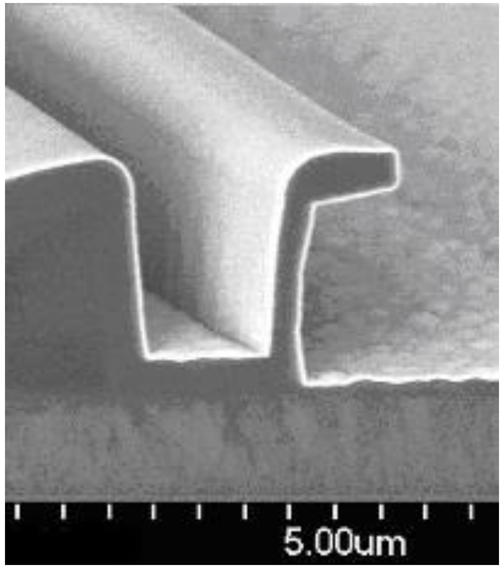
Manufacturing sample CMOS pressure sensor

High-precision readout ASIC

Encapsulation

ALD as encapsulation layer for implantable sensors

- Example: Pressure sensor for medical applications
- Passivation Requirements: Hermetic close, biocompatible, consistent against chemicals / humidity, low mechanical influence, (protection against light)
- Used materials: nano laminate of different metal oxides
- Cooperations with industrial partners:
    - 1x clinical trials (done)
    - 2x animal trials (planned)



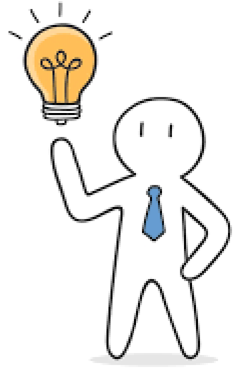
Passivation stack out of Al_2O_3 + Ta_2O_5

ALD encapsulation can also be used for other applications

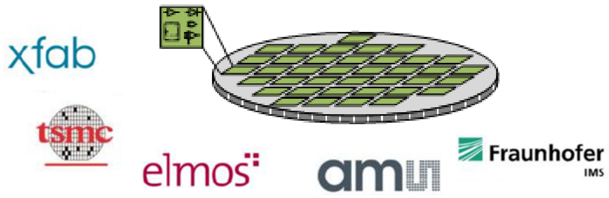
- General protection against humidity
- Protection against harsh environments, e.g. corrosive gases
- …

How to collaborate

Our benefits



- We have experience across the entire process chain
  - Idea discussion
  - Support in concept development
  - Layout creation
  - Collaborative process development with the option to start on different substrates
  - Experience in integration including readout electronics and telemetry
  - From Lab to Fab: Capability to scale the process up to pre-series, including passing through relevant quality gates
  - If needed, we also assist with transfer to one of the larger fabs



- We can adapt to customer requirements
  - We successfully collaborate with startups and can respond with the necessary flexibility
  - Possibility of offering single process steps
  - Possibility of developing full process flows

How to collaborate

Cooperation models

- Feasibility study
    - Analyzing the requirements
    - Developing possible technological solutions
    - Presenting the results in a joined Workshop

- R&D projects
    - Developing your process ideas

- Technology Services
    - Taking over individual process steps
    - Possibility of developing this process step
    - Possibility of tuning our tools to your specifications

- Public funded projects
    - E.g. EU-Projects

Contact

Dr. Dorothee Deschmann
dorothee.deschmann@ims.fraunhofer.de

Fraunhofer Institute for Microelectronic Circuits and Systems IMS
Finkenstr. 61
47057 Duisburg
www.ims.fraunhofer.de/en.html