FAMES
greener electronics
FD-SOI · NVM · 3D · RF · PMIC

The FAMES Pilot Line

Dominique Noguet, FAMES Project Coordinator – CEA-Leti

Chips JU

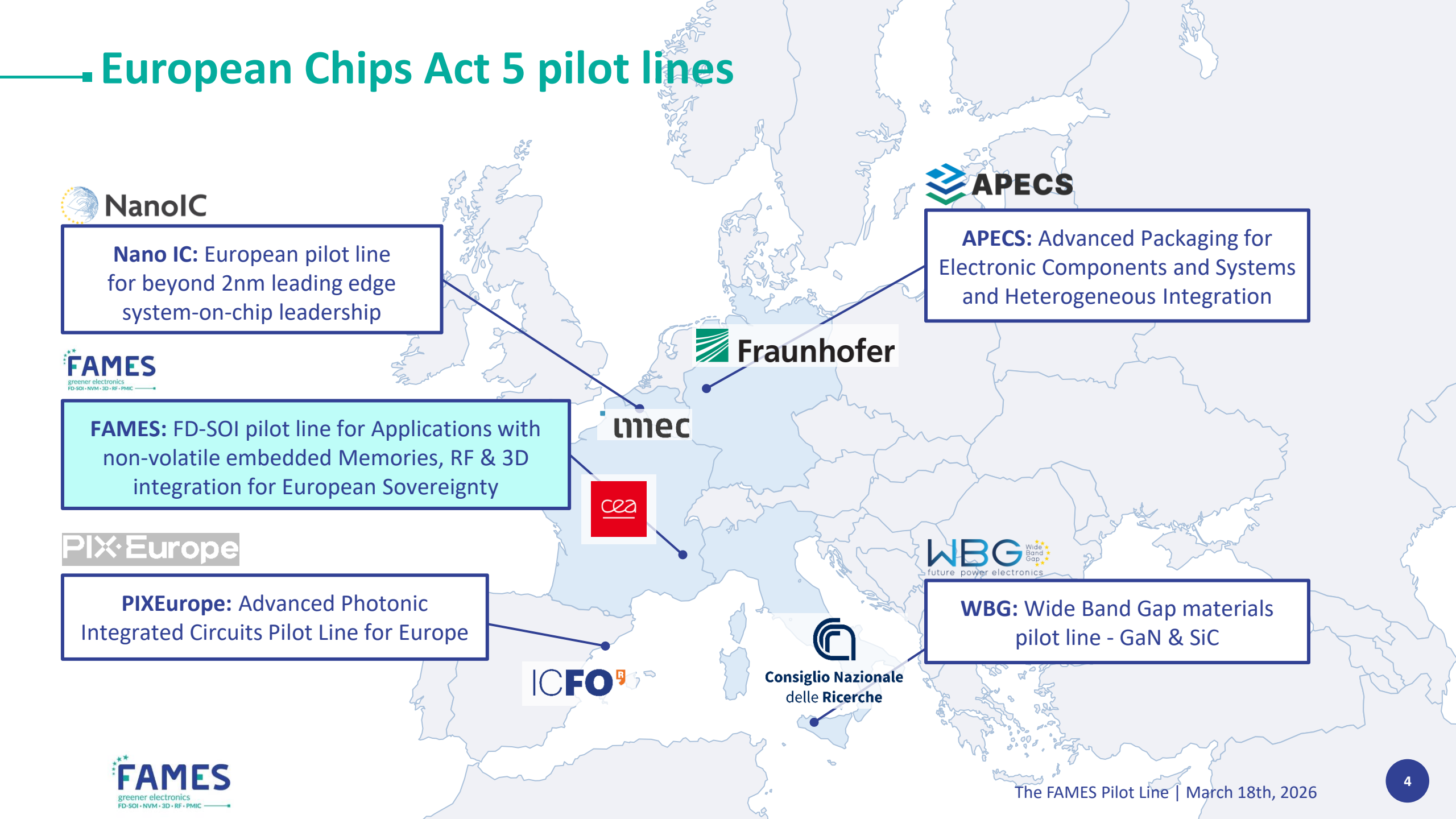
Outline

1. Chips JU Pilot Lines, and FAMES at a glance
2. FAMES Key Activities and Technologies
3. How to reach us?

Chips JU Pilot Lines

FAMES at a glance

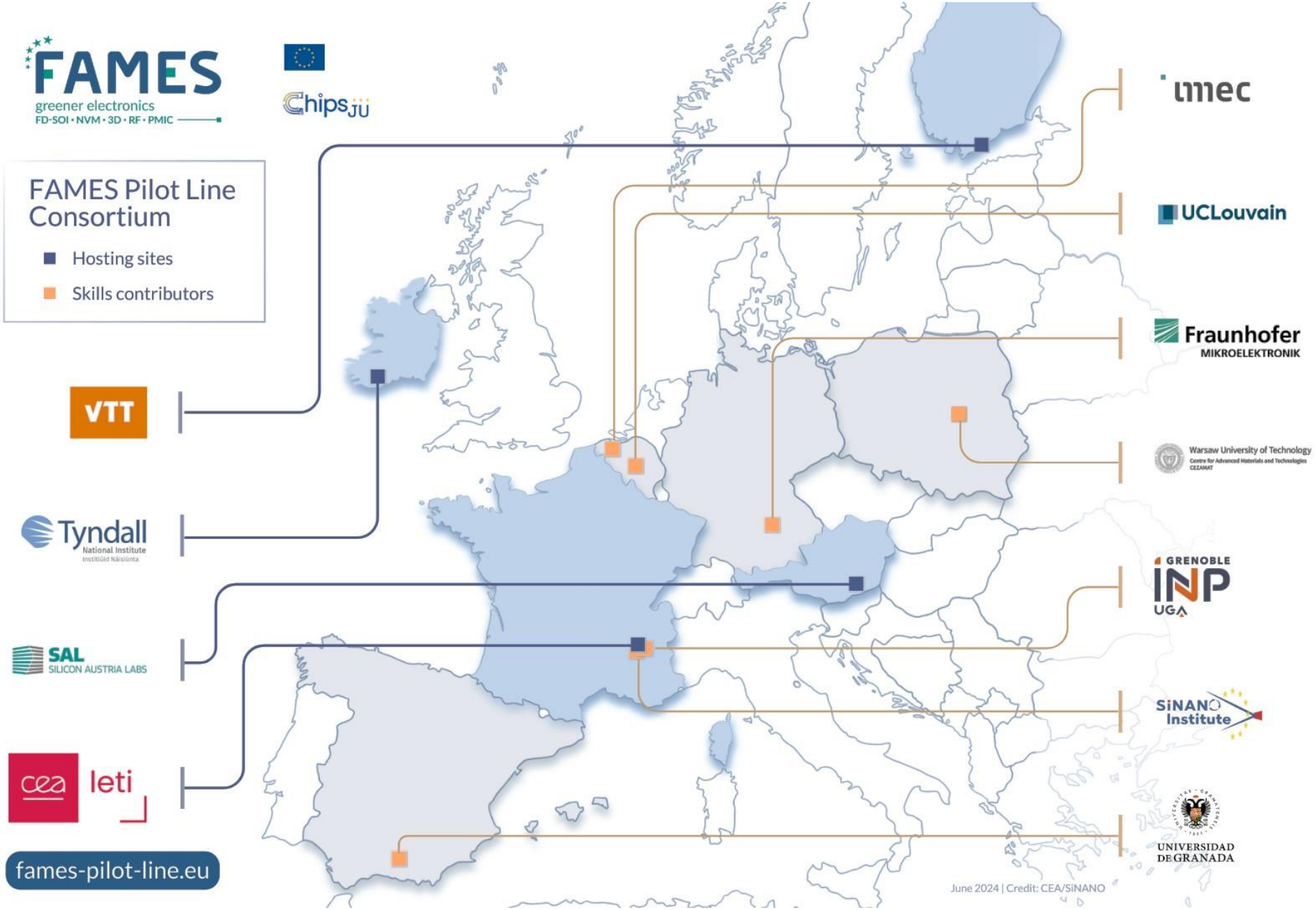
European Chips Act 5 pilot lines



Budget : €830 M
- CAPEX: €382 M
- OPEX: €448 M

Funding mechanisms
- 50% Chips JU
- 50% Member States

Dec. 2023 → Dec 2028



Aim of FAMES

- A European semiconductor pilot line for advanced technologies
- With opportunities for disruptive chip architectures, performance improvements and significant energy savings
- Strengthening European leadership in advanced semiconductors and opening new economic opportunities for a wide spectrum of markets

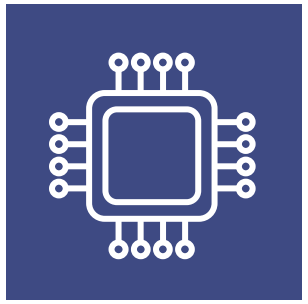
Credits: Jayet/CEA

Opening the pilot line to European stakeholders

44 letters of support

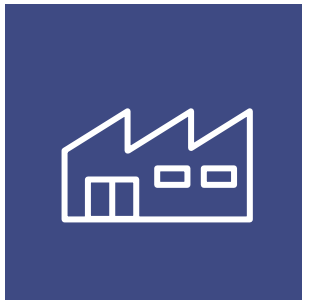
FAMES Key Activities

FAMES Key Activities



R&D

5 Technologies + an eco-innovation Program



Pilot line implementation

Cleanroom equipments

Open-access

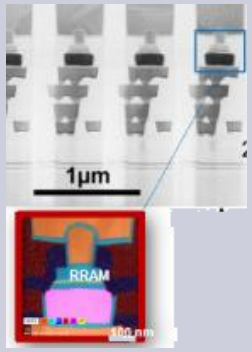
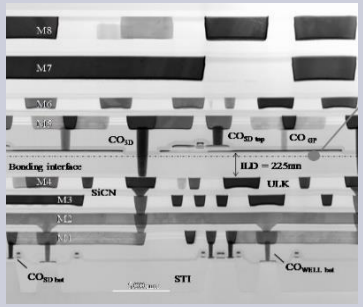
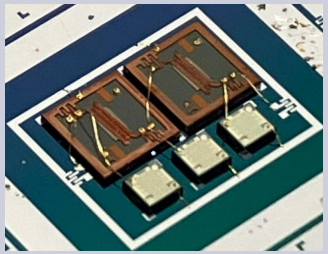
Yearly Calls Spontaneous Requests

Training & education

Workshops, webinars and schools

FAMES Technology Portfolio

FAMES Technological Portfolio

FD-SOI	Embedded non-volatile memories	Radiofrequency components	3D integration	Small inductors for DC-DC converters	Eco-innovation
10 nm and 7 nm nodes	OxRAM, FeRAM, MRAM and FeFET	Switches, filters, and capacitors	Heterogeneous and sequential	Power management integrated circuits (PMIC)	
					
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Innovative, Differentiated Developments for Key Markets

Computing

- Microcontrollers
- MPU
- Trusted IC
- AI/ML chips

Sovereignty fields

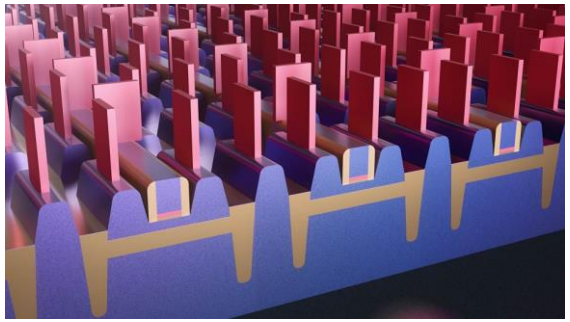
- Quantum chips
- CryoCMOS chips
- Trusted IC
- New space components

More Than Moore

- Automotive
- 5G/6G chips
- RF connectivity
- Smart sensors
- Smart imagers
- Smart displays
- IoT devices
- Cybersecurity
- Wearables

FD-SOI

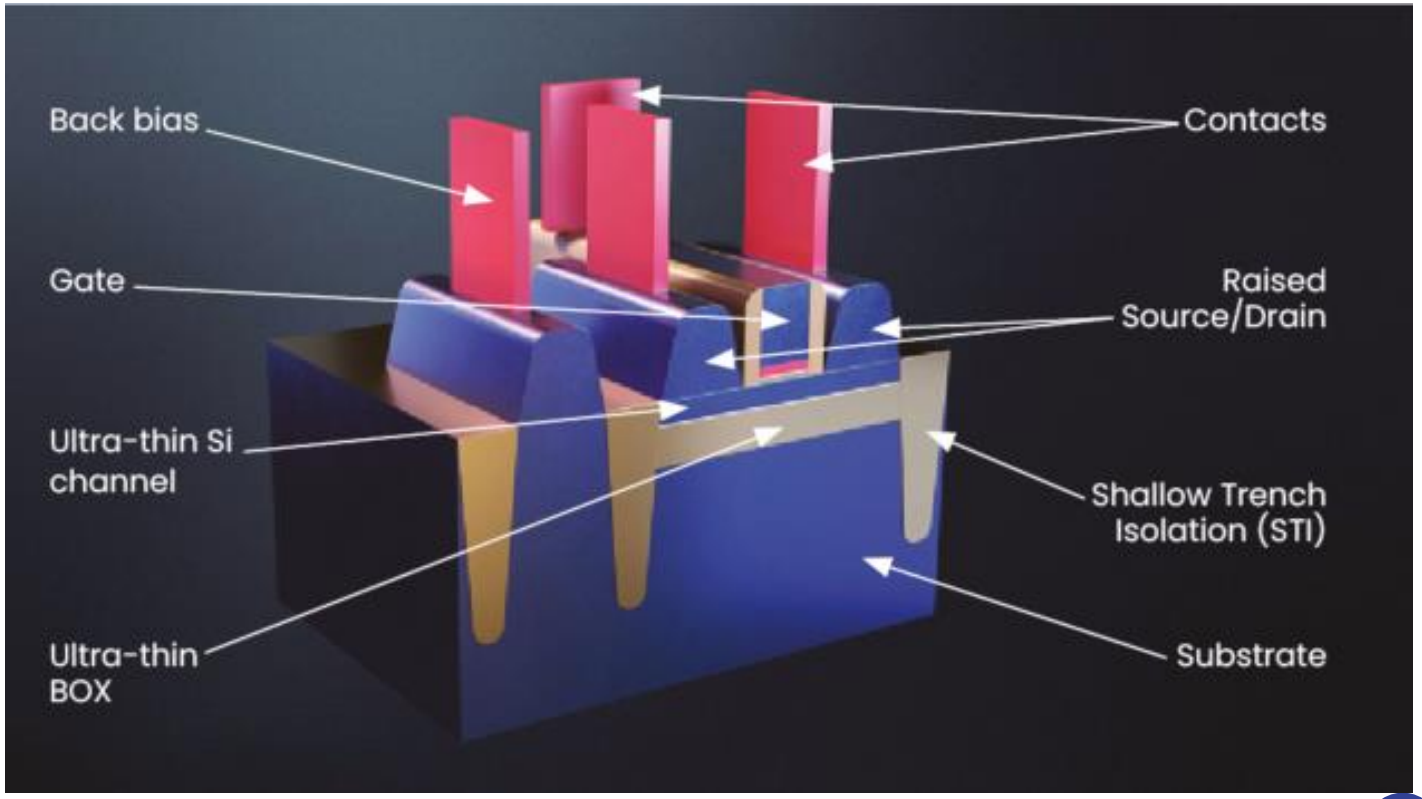
FD-SOI 10nm and 7nm nodes



An innovative generation of chips with the best balance in Power, Performance, Area, Cost and Environment (PPAC-E) for highly energy efficient applications

- Transistor density
- High-performance/low-power trade-off
- Reduced current leakage
- Manufacturing costs
- Radiation resistance

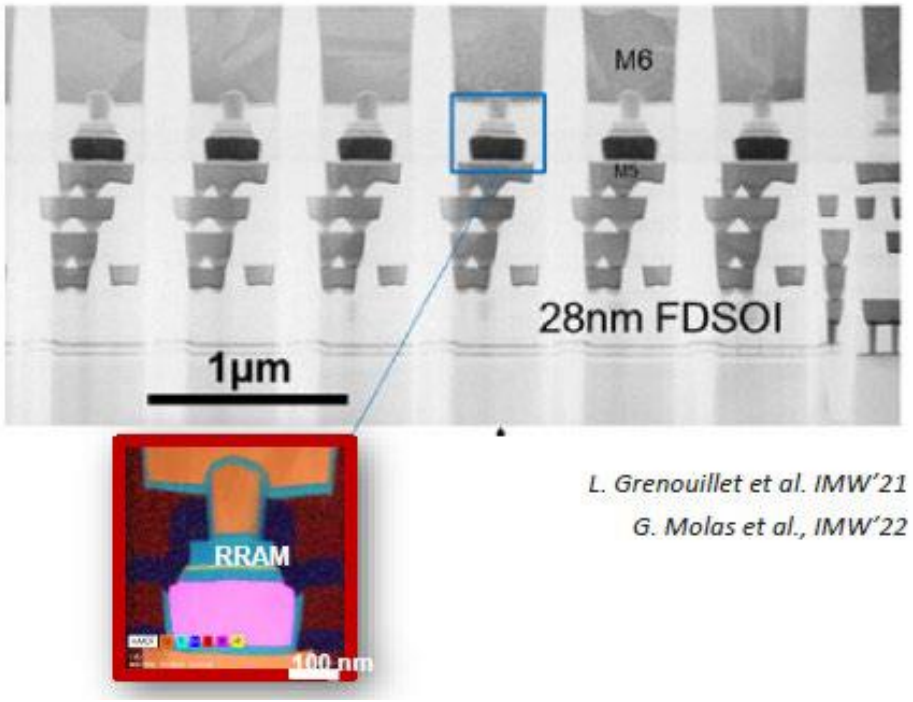
- Over **150 patents** filed by CEA-Leti



FAMES greener electronics FD-SOI · NVM · 3D · RF · PMIC

eNVM

Emerging Non-Volatile Memories embedded in the BEOL



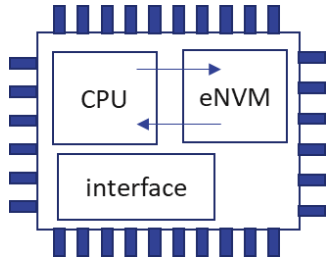
L. Grenouillet et al. IMW'21
G. Molas et al., IMW'22

EMBEDDED quicker access time and lower power compared to stand alone as they are on chip close to the logic

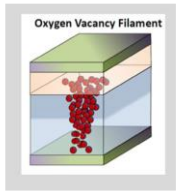
NON VOLATILE retaining data even when the power is off

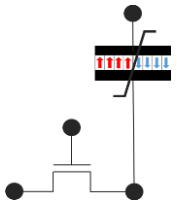
PERFORMANT reprogrammable and erasable multiple times, faster to write compared to Flash memories

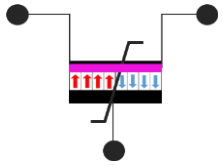
LOW POWER lower power consumption than external non volatile memories



OxRAM **MRAM** **FeRAM** **FeFET**





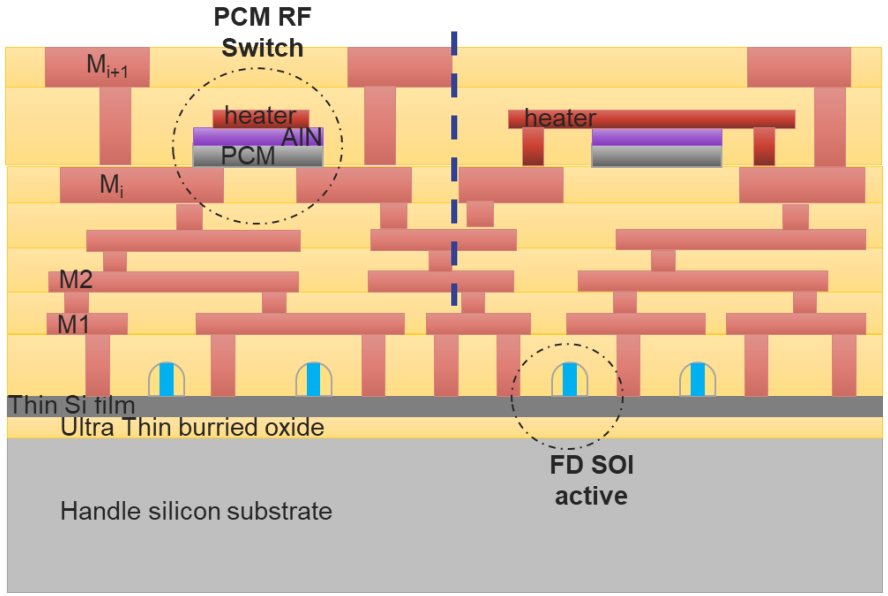


RF components

RF components integrated in the BEOL

FD-SOI is well-suited for RF/analog and mixed signal circuits

- **Performance/power savings**
- **Covering a wide frequency range**
- **From a few GHz up to the D-band centered at 140 GHz**

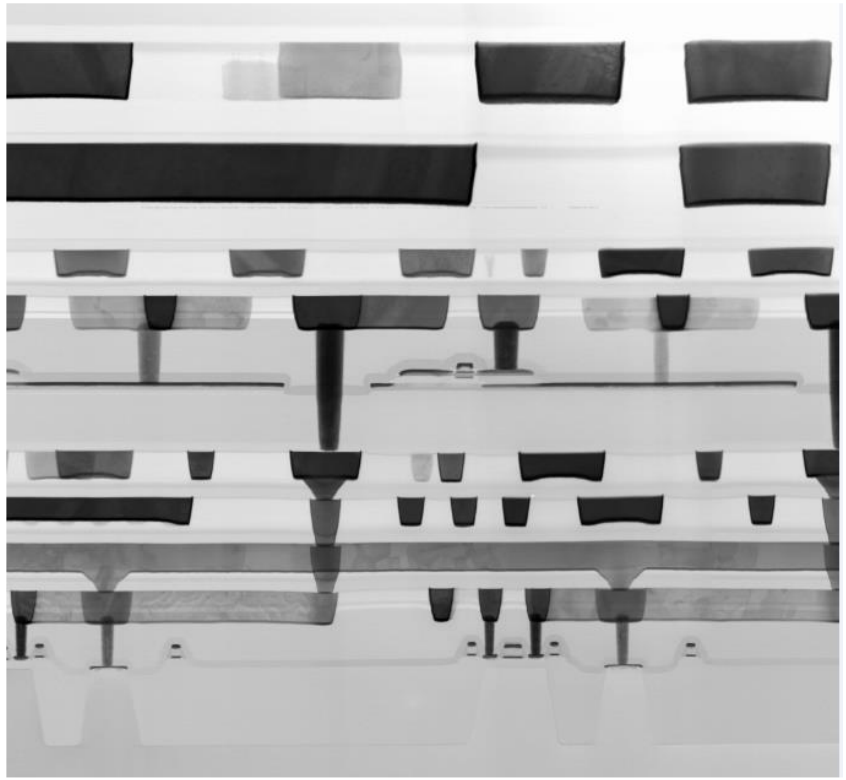


FAMES → RF active and **passive components**, to enrich the FD-SOI CMOS technology offer and open new markets:

- **RF switches based on Phase Change Materials**
- **RF acoustic filters**
- **RF magnetic-based miniaturized circulators for >GHz bands**

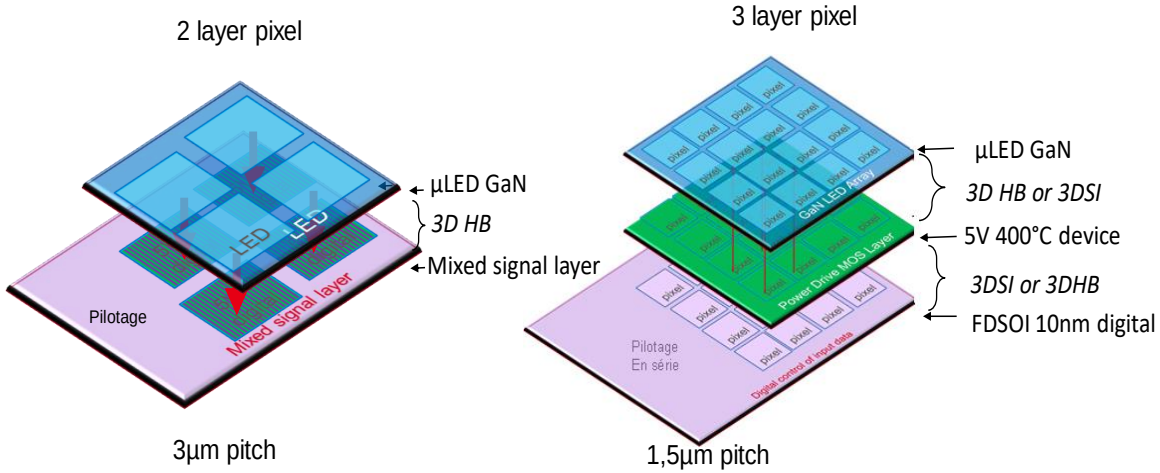
3D integration

3D Sequential integration



FAMES aims to enlarge FD-SOI heterogeneous co-integration with other devices using 3DSI to address new systems and markets

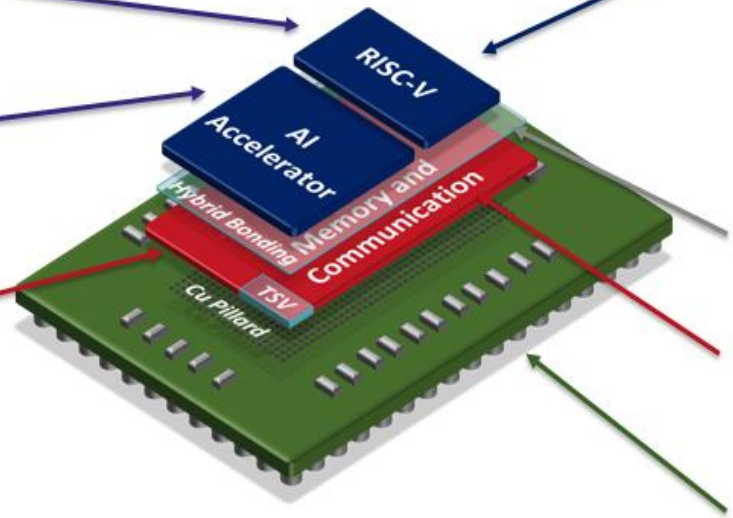
- Demonstrate 3D sequential integration with increasingly complex circuits;
- Evaluate opportunity of Smart and scaled 3tier-pixels with GaN µLED and RF applications



Edge computing based on 3D hybrid bonding (HB) chiplet architecture

Architecture

- **Generic Computing with OpenHW**
- **Low power accelerator**
- **Chassis die** with peripherals, IOs, memory and communication infrastructure



Technology

- **Multi-chiplets:**
  - Advanced technology node
  - Heterogeneous (size, technology node, pitch)
  - Face down
  - No TSV
  - Full digital compute chiplet
- **Hybrid bonding:**
  - Die-to-wafer, Face-to-face
- **Base die:**
  - Mature technology node
  - TSVs for power delivery and IOs
  - Face-up
- **Package**

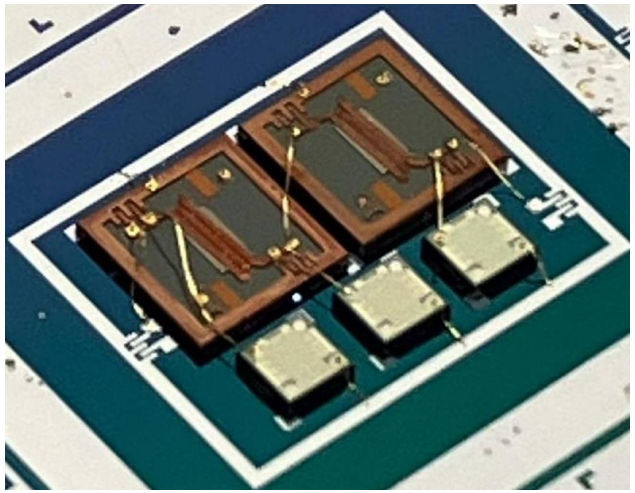
Novel 3D approach developed by FAMES:
Chiplet architecture with very low latency

- TSV : Back-Side Mid-BEOL TSVs
- Cu/SiO2 HB : 5 µm pitch
- Front-Side and Back-Side RDLs

→ **To increase interconnect density by a factor of up to 100**

Integrated Magnetics & Power Management IC

Integrated Magnetics and PMIC for DC-DC power conversion



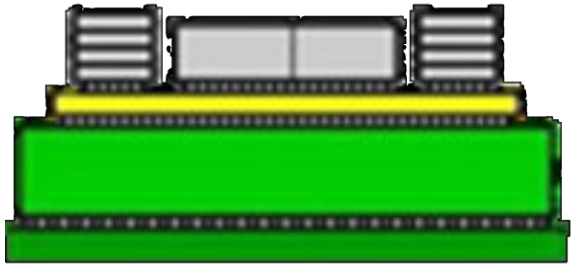
Power management integration in Systems-on-Chip

- Power converters densely co-integrated with digital or RF loading blocks
- Solutions to improve **power delivery** in chiplet architectures
- **Integration of passive components close to SOC**
- Design and fabrication of **integrated magnetics for inductive passive** components

FAMES will provide solutions to improve power delivery by integrating passive components into SOC

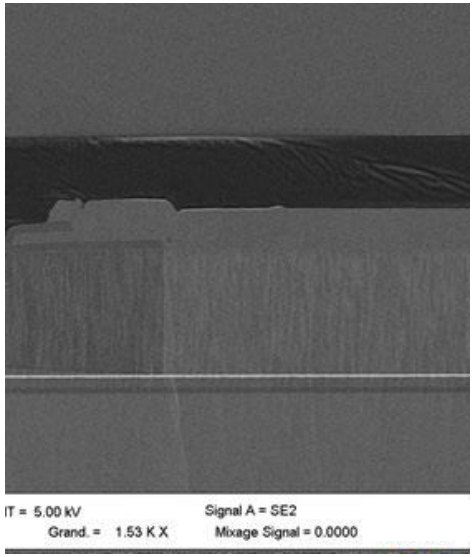
- Design and fabrication of integrated magnetics for inductive passive components
- Collective assembly of passives by Micro Transfer Printing (MTP)
- Performance assessments via a functional technology demonstrator that integrates an inductance-based DC-DC power converter, for granular power delivery

Power conversion: 3D caps

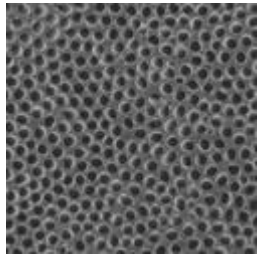


Hybrid integration

Hybrid integration of high density capacitors and CMOS power conversion stages on 300mm wafers for advanced 6G systems and HPC applications



Higher surface capacitors



High A/R MIM

- Very high density capacitors:
  - Specific ALD method developed for a MIM deposition with aggressive aspect ratios
  - TiN bottom and top electrodes
  - Si oxide and/or alumina for dielectrics

A game-changer for power signal management

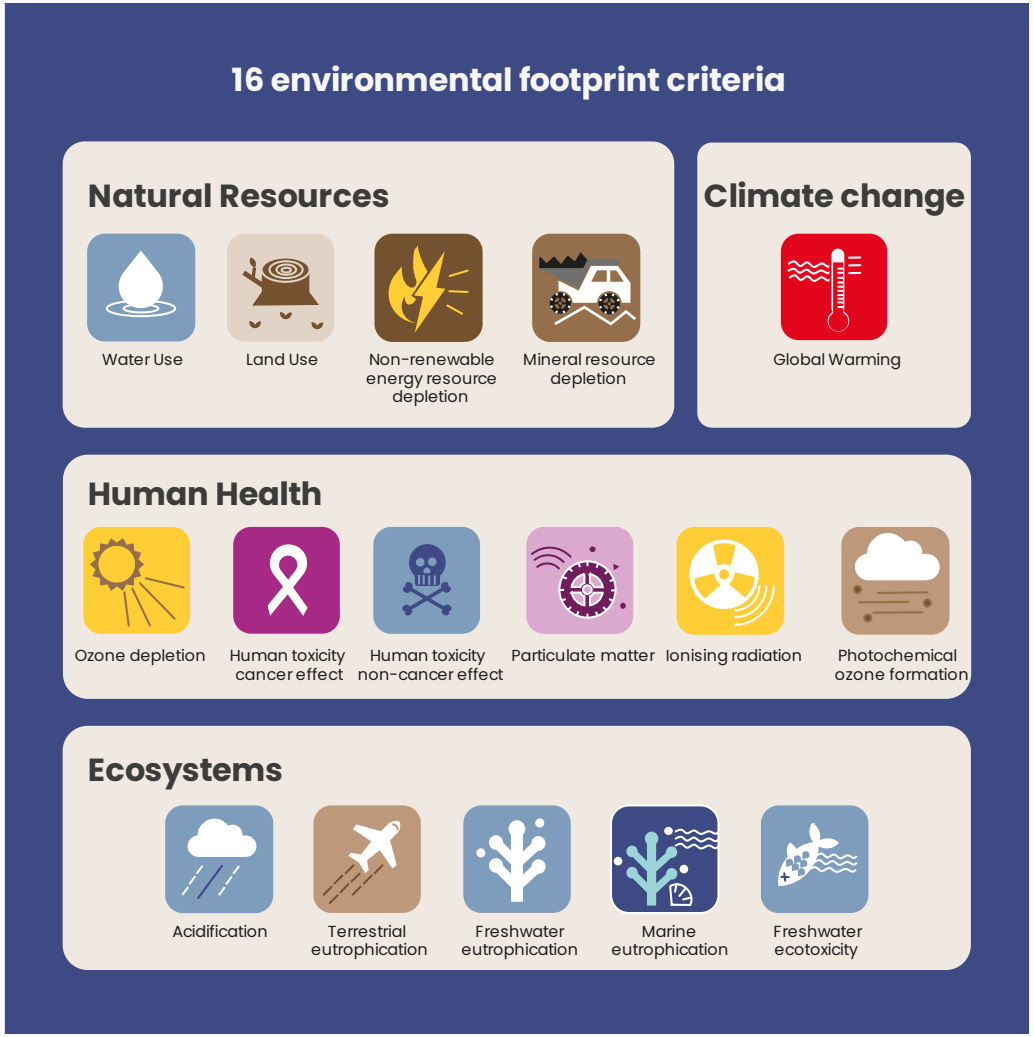
Eco innovation

FAMES Eco Innovation Offer

Eco-innovation for more sustainable electronics
Reducing the impacts of electronics through R&D

- The development and implementation **of lifecycle analysis (LCA)**
- The validation of eco-innovative solutions in a production-like environment
- The development of technologies and end-to-end systems to meet specific environmental criteria for identified use cases.

16 environmental footprint criteria



Pilot line implementation

New facility and Pilot Line tool capability in Europe

New cleanroom at CEA-Leti
2000m² double basement state of the art facility

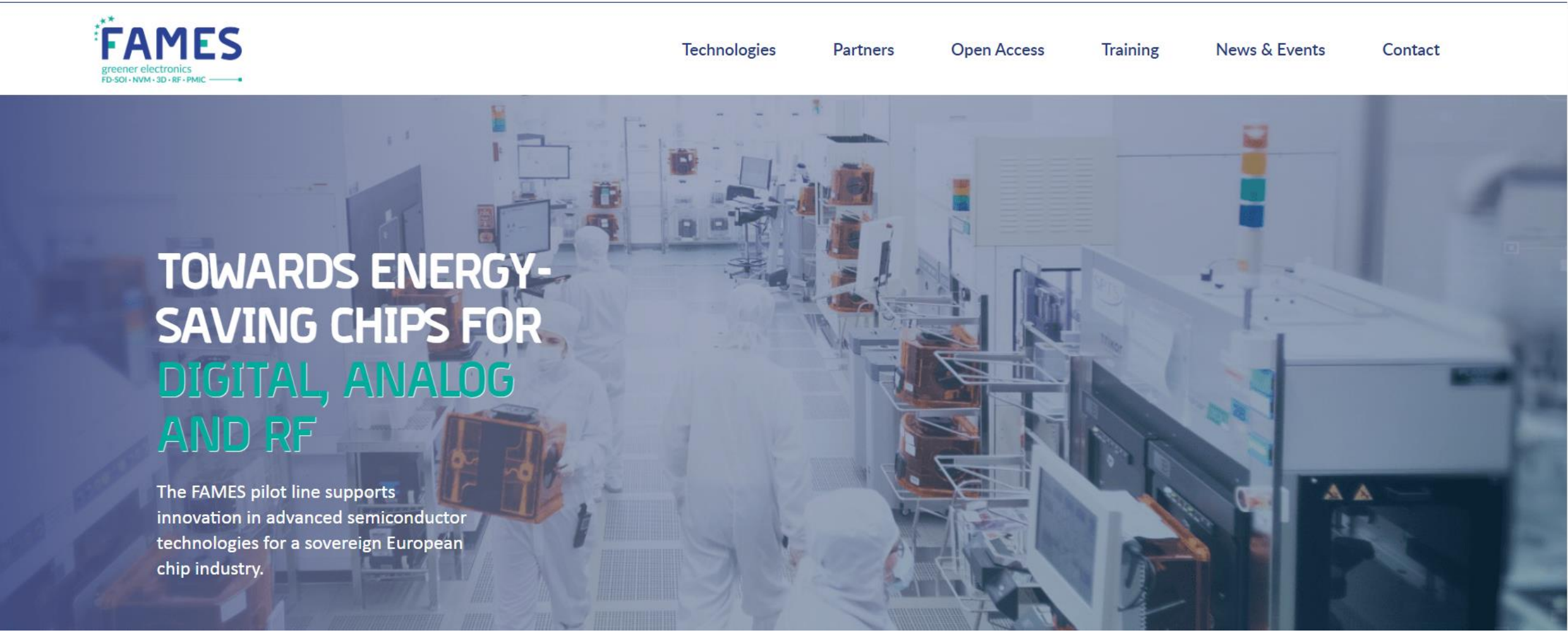
Procurement of 100+ pieces of equipment planned by the Pilot Line on 4 hosting sites

- France
- Finland
- Ireland
- Austria

NextGen
ANR-22-NEXG-0001

How to reach us?

FAMES Pilot Line website



https://fames-pilot-line.eu/

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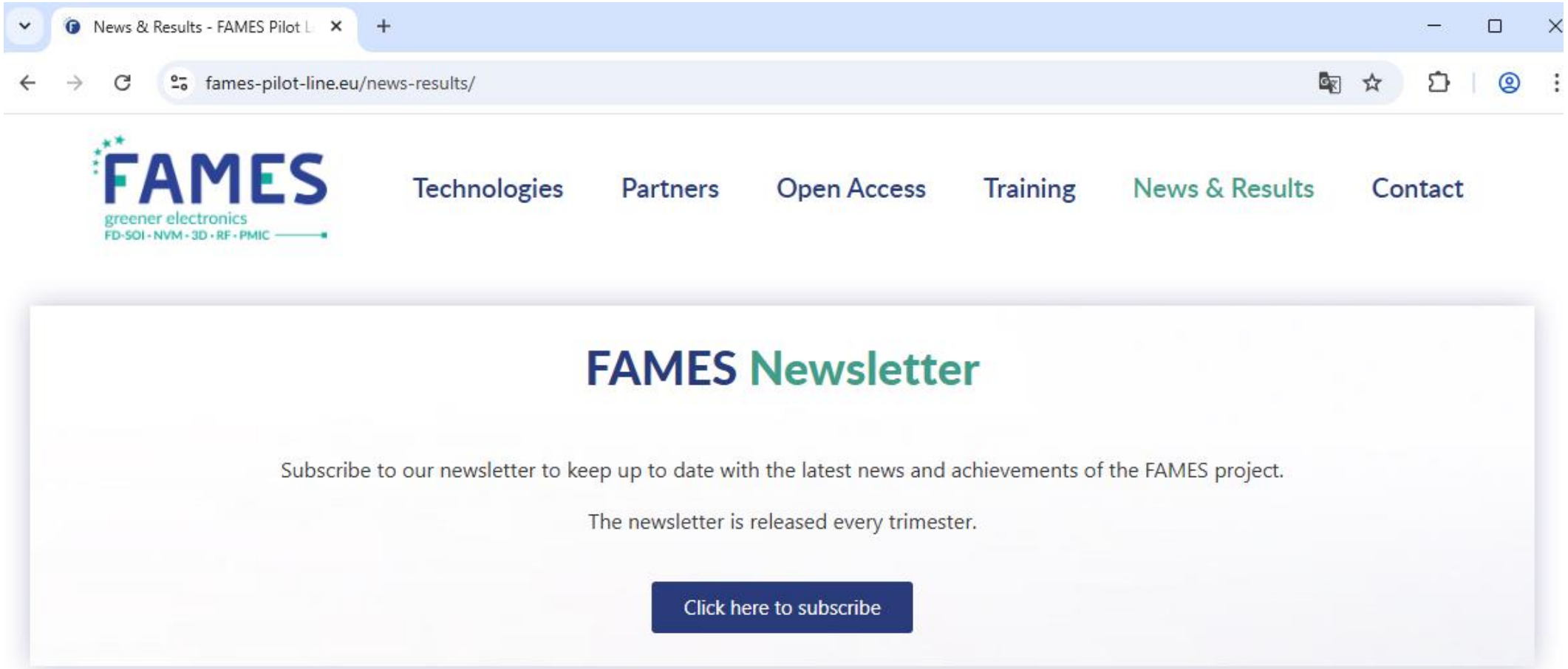
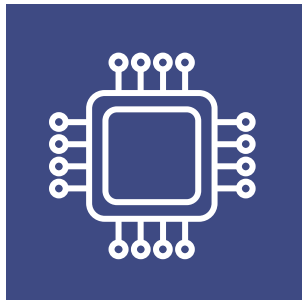
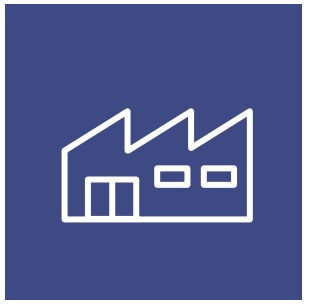


FAMES Key Activities



R&D

5 Technologies + an eco-innovation Program



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(2023 – 2028)

Sponsors

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Co-funded by the European Union

Chips JU

FRANCE 2030
NextGen
ANR-22-NEXG-0001

BUSINESS FINLAND

Ministry of Science and Higher Education
Republic of Poland

GOBIERNO DE ESPAÑA
MINISTERIO PARA LA TRANSFORMACIÓN DIGITAL Y DE LA FUNCIÓN PÚBLICA

PERTE Chip

Das Land Steiermark

Member of UAR INNOVATION NETWORK

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Bundesministerium Klimaschutz, Umwelt, Energie, Mobilität, Innovation und Technologie

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Vlaamse overheid

Wallonie recherche SPW

FFG
Promoting Innovation.

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Thank you

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