

NanoIC

Accelerating beyond-2nm chip innovation across Europe

GIUSEPPE FIORENTINO, Program Manager, imec

Co-funded by
Chips JU

What is the NanoIC pilot line ?



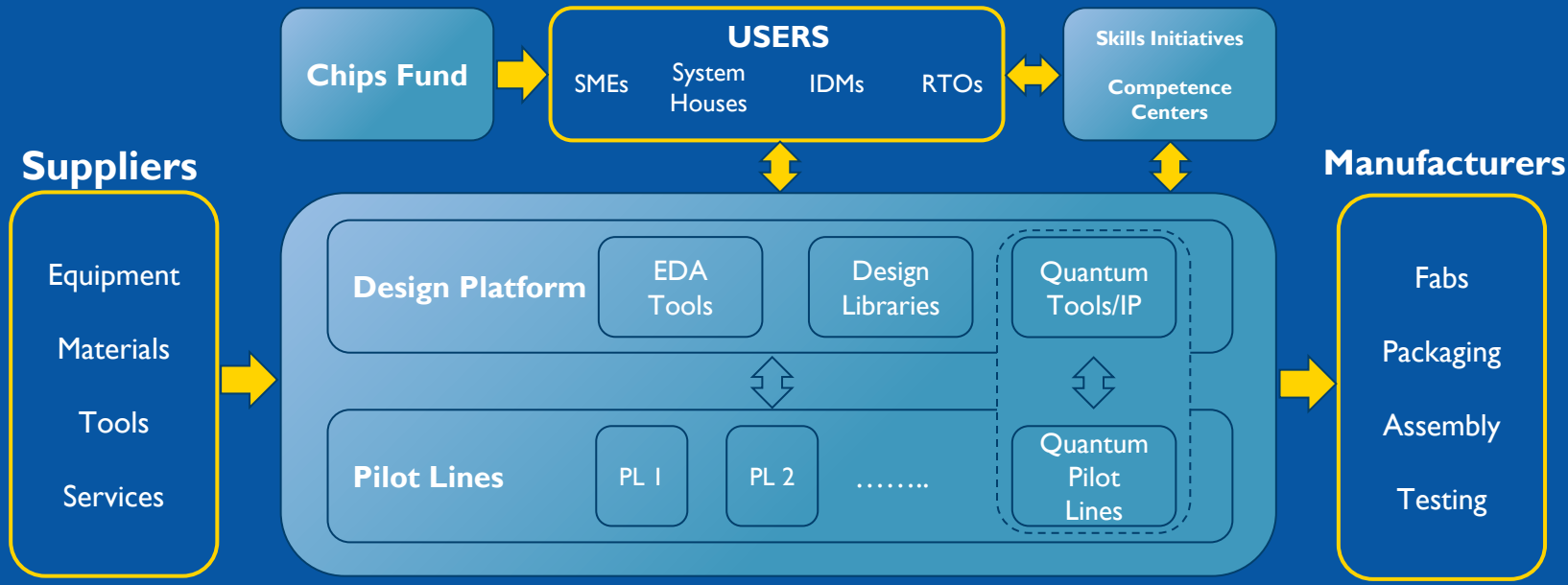
NanoIC will provide Europe with a **beyond-2nm** leading edge system-on-chip pilot line.

It will develop advanced **logic**, novel **memories** and advanced **interconnect** technologies.

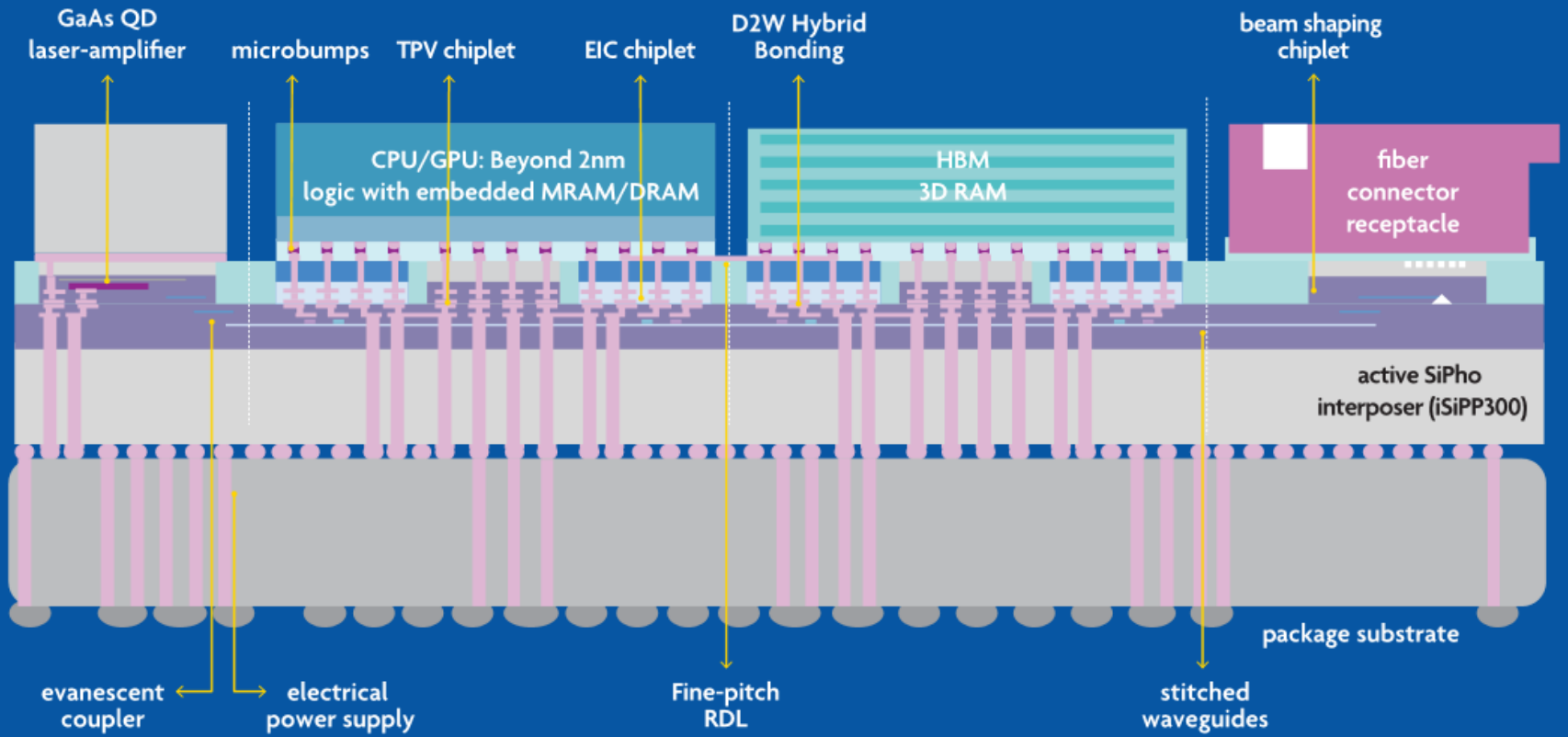
- Infrastructure & Equipment
- Technology Development
- Access & Selection
- Education & Workforce Development

imec · cea leti · Fraunhofer MIKROELEKTRONIK · Tyndall National Institute · VTT

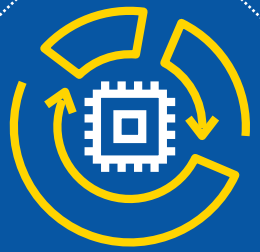
Relationship of NanoIC Pilot Line with other Chips JU initiatives



Future HPC system concept leveraging NanoIC technologies



Technology platforms in NanoIC scope:



ADVANCED INTERCONNECTS

3D D2W, 2.5D FP RDL,
Si interposer, Integrated III-V lasers
Fabrication services

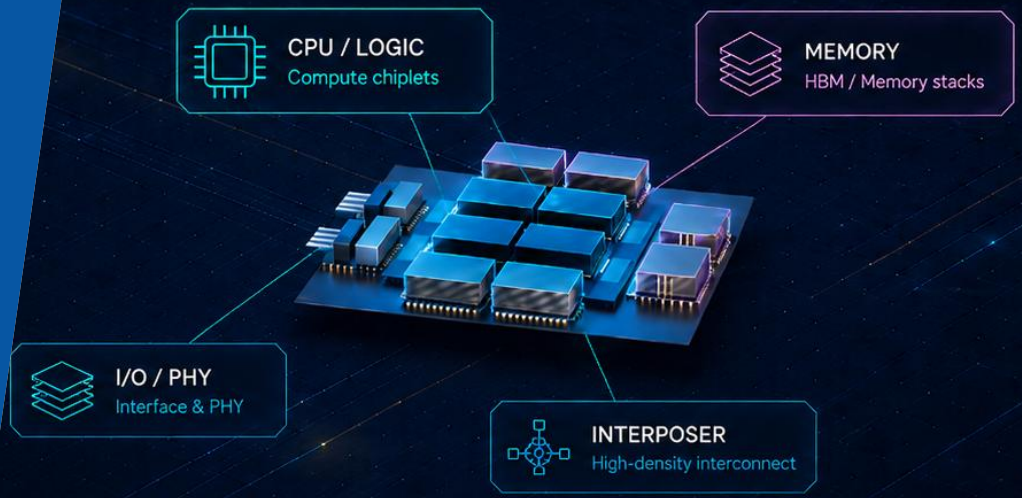
NOVEL EMBEDDED MEMORIES

SOT-MRAM,
eDRAM,
3D memory platform
Fabrication services

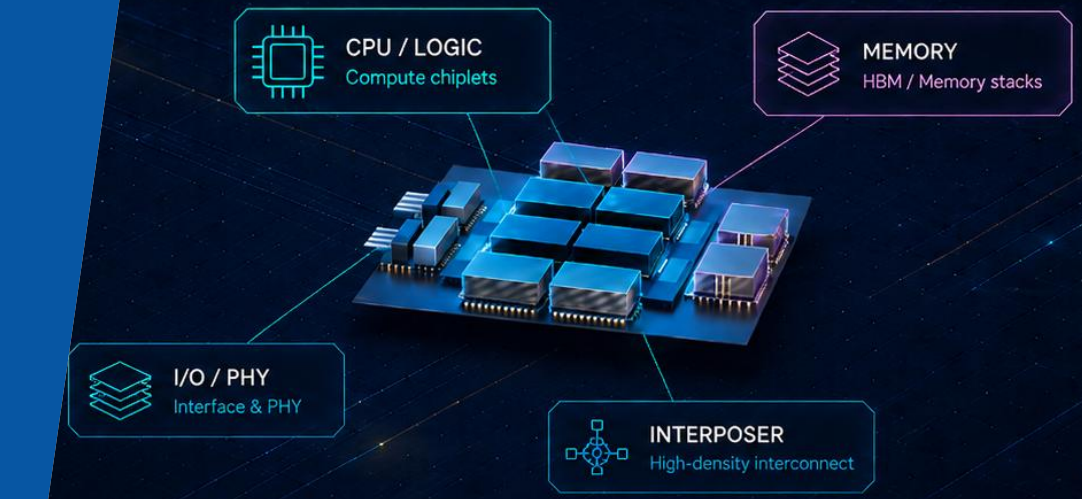
ADVANCED LOGIC

Virtual PDK : Nanosheets targeting 2nm (N2), A14 and A10 technology nodes, CFETs targeting A7 node, High NA EUV

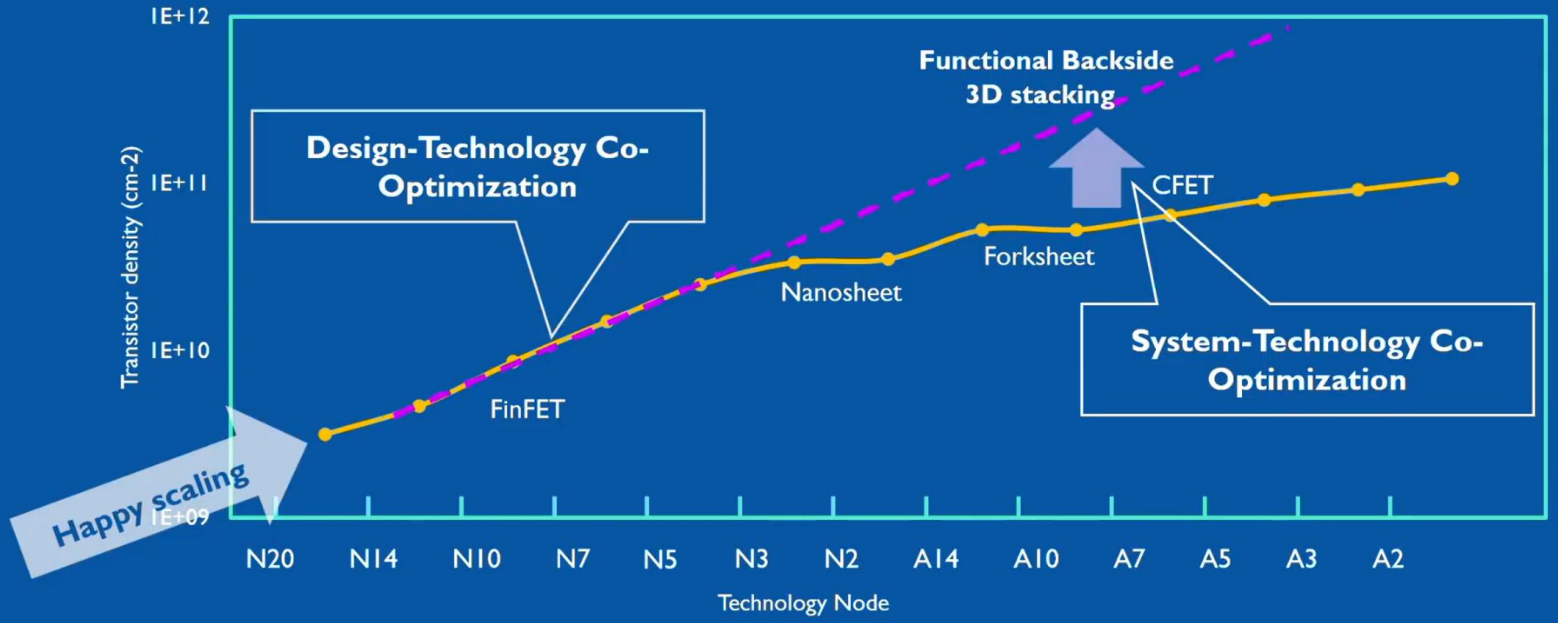
NanoIC Pilot Line Technology offers



Advanced Logic



Logic scaling



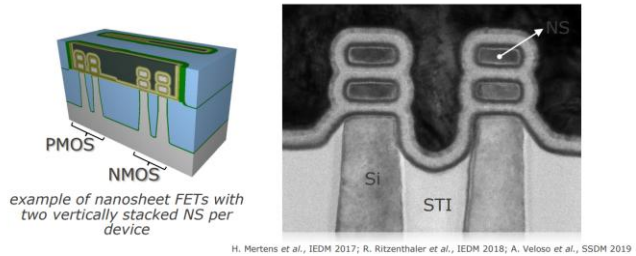
N2 and A14 Technology P-PDKs

- Digital standard cell libraries (100+ cells), GDSII layout, Abstracted layout views
- Timing/power views, Multi-VT, Standard cell SPICE netlists, VT corners support
- Backside connectivity EDA technology files (BSPDN)
- 60+ Access requests already received, 24 already granted

Now available

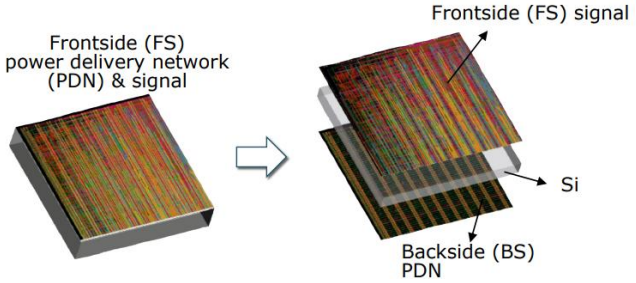
- SRAM Macros integration,
- Extended VDD support,
- Improved TCAD models calibration on temperature scaling

- A10 and CFET Pathfinding PDKs available at a later stage

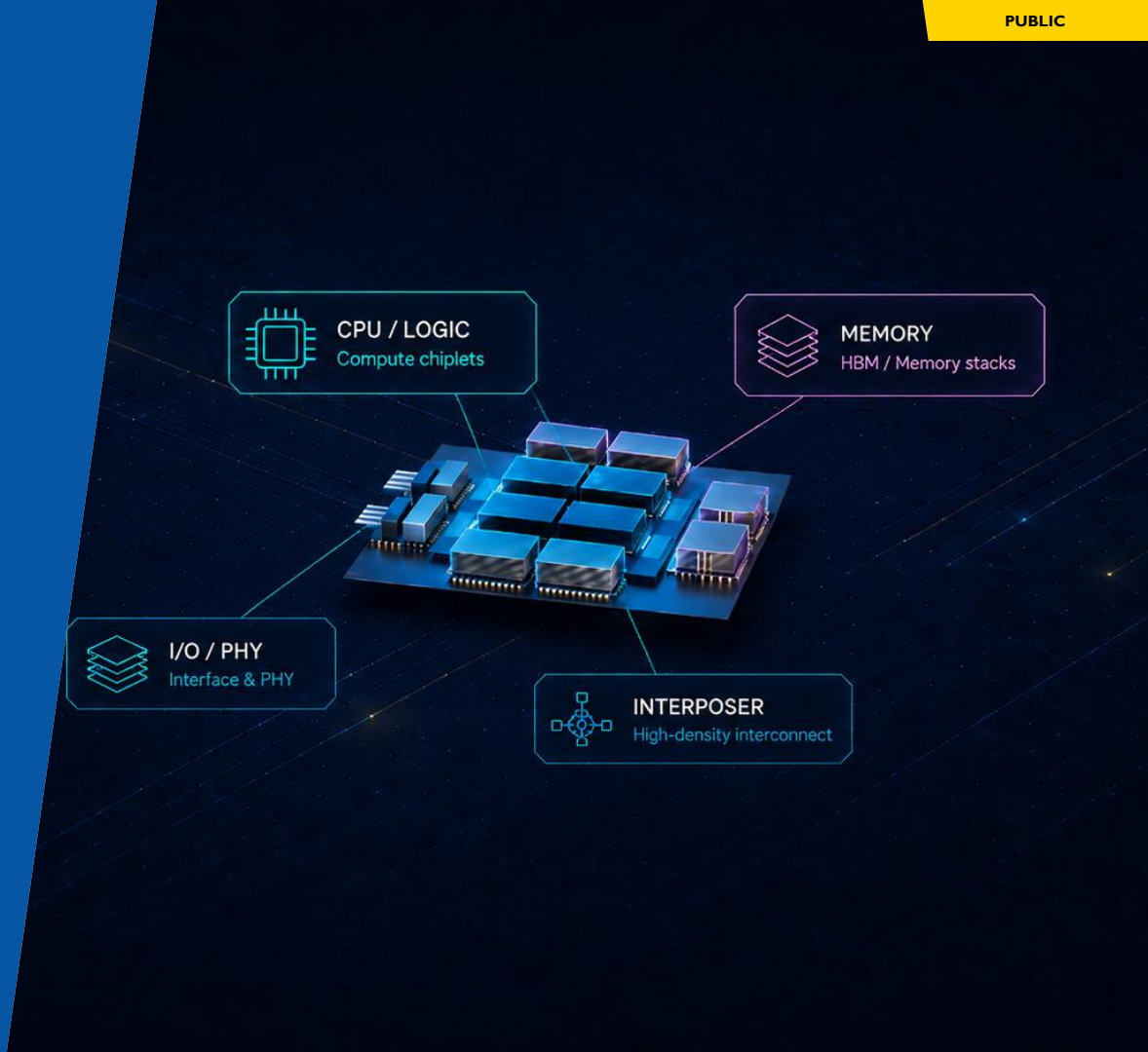


example of nanosheet FETs with two vertically stacked NS per device

H. Mertens *et al.*, IEDM 2017; R. Ritzenthaler *et al.*, IEDM 2018; A. Veloso *et al.*, SSDM 2019



Embedded Memories

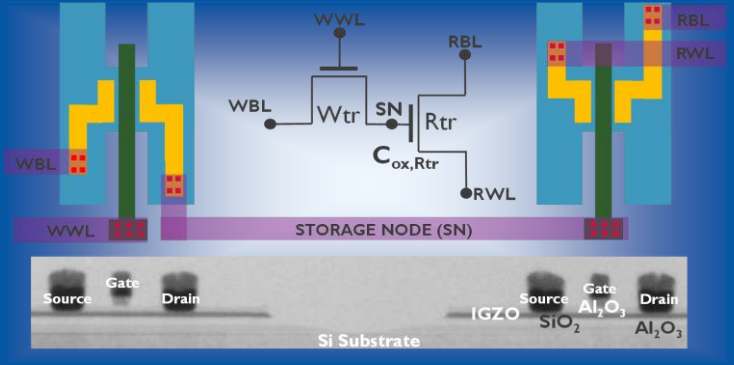


EDRAM Technology – P-PDK

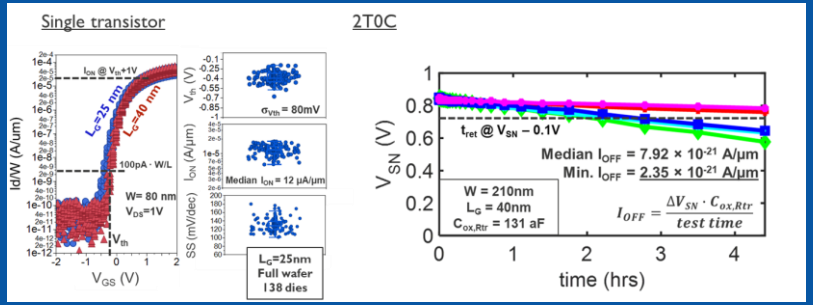
Embedded memory macro for cache applications

- Models calibrated using IGZO device experimental data, ensuring realistic behavior for early-stage design exploration.
- Including IGZO eDRAM bitcell architectures, chosen through early Design-Technology Co-Optimization (DTCO) efforts.
- Bitcell models complemented with extracted parasitic based on N40 or N7 design rules, and can be combined with third-party CMOS front-end technologies supplied by the user.

Latest results show excellent retention achieved on side-by-side 2T0C*



*Capacitorless eDRAM is now considered one the most promising candidates for **AI applications***



A. Belmonte et al., SNW 2025

NanoIC

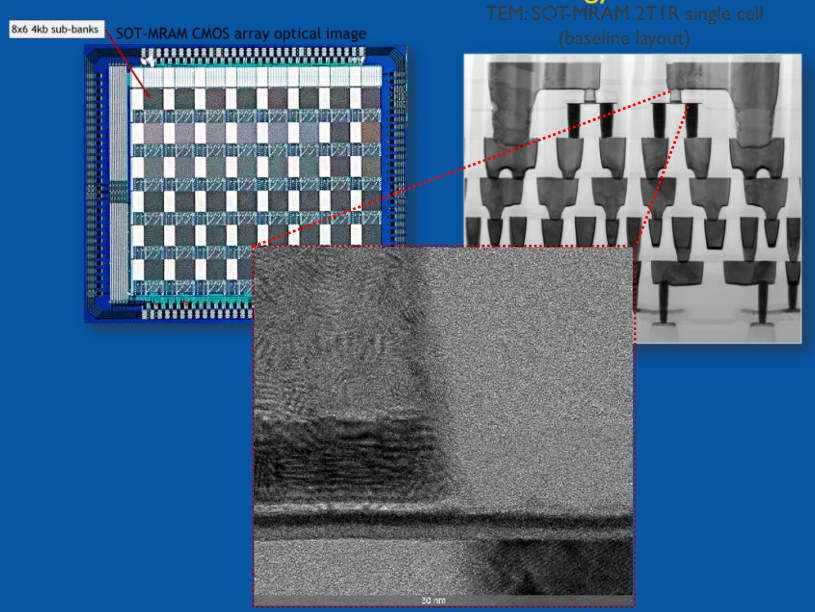
Co-funded by Chips JU

The NanoIC vision on Spin Orbit Torque MRAM

Embedded memory macro for cache applications

- Establish an **SOT-MRAM** process flow on the NanoIC pilot line
- SOT eMRAM Pathfinding PDK available for academia, LEs, SMEs, startups at a later stage

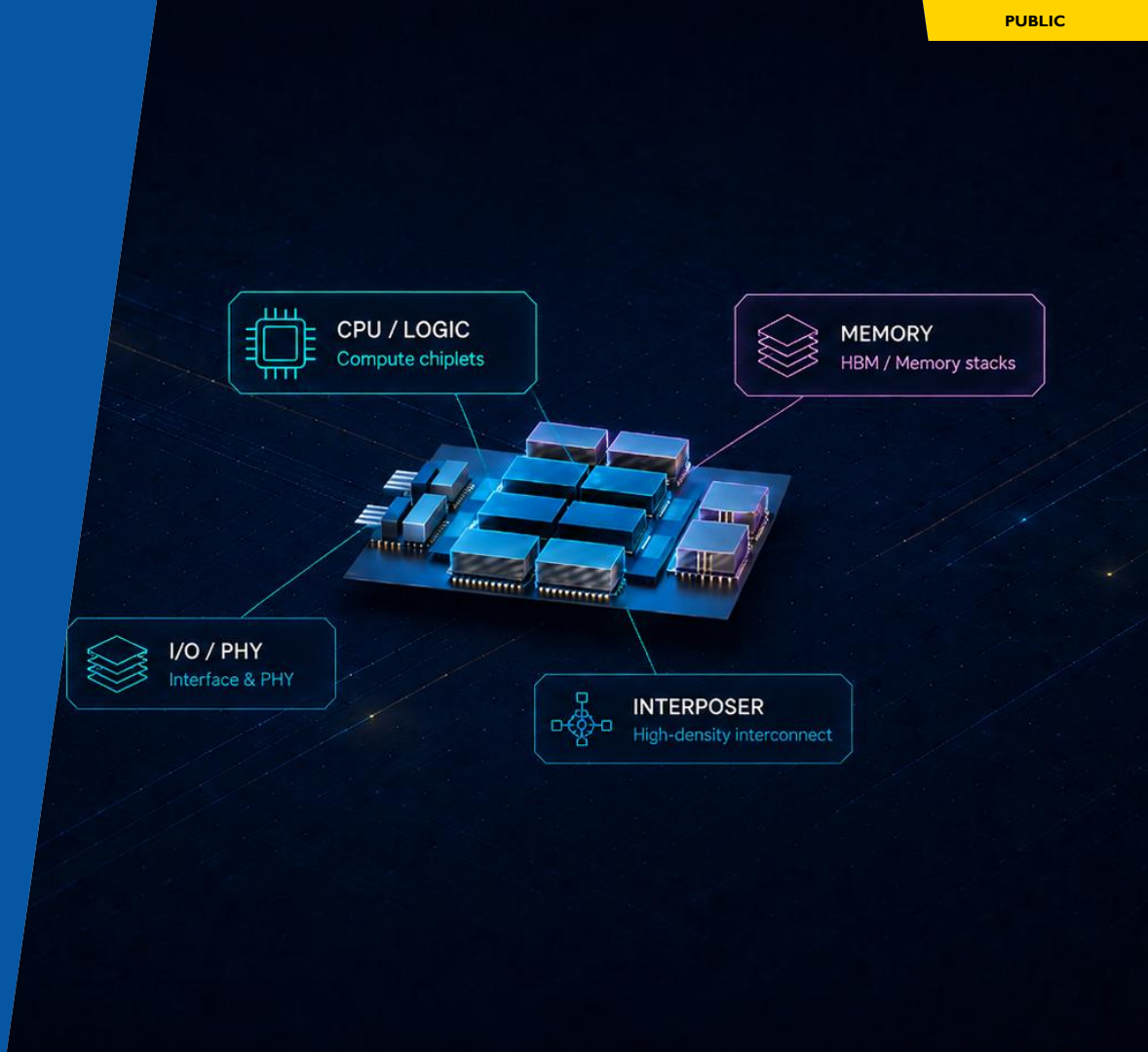
eSOT-MRAM will be integrated on **40nm CMOS** technology



Latest results show excellent read/write and retention (>10 yrs) properties

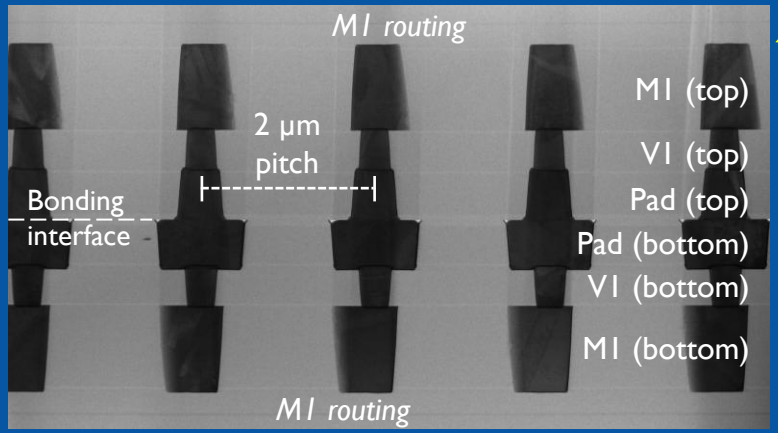
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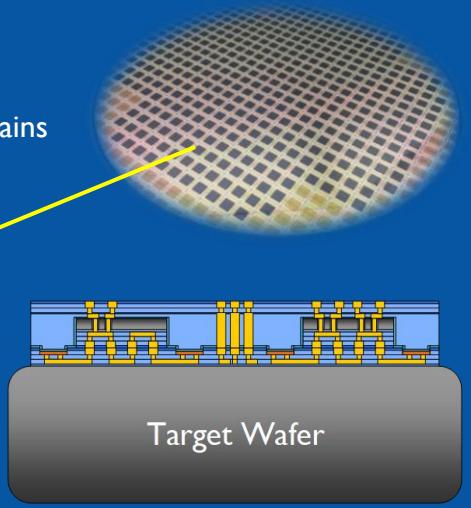
Advanced Interconnect



D2W Hybrid bonding : 2µm pitch interconnect enablement

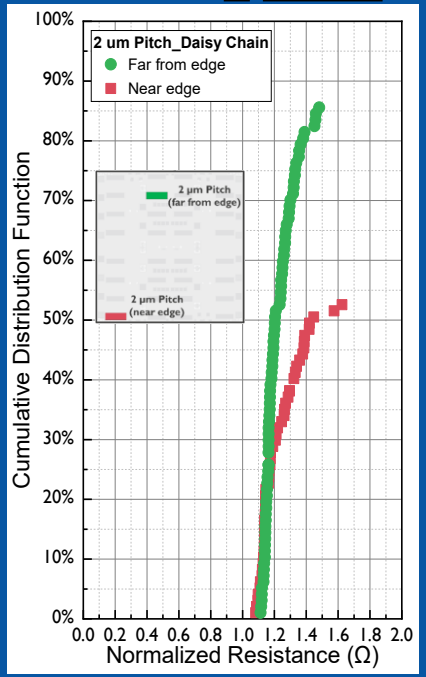
- Pathfinding PDK available as of Feb.2026
- Cu-Cu/Oxide bonding
- Required topography variation < 1 nm/um
- Towards platform flow for prototyping : 90% Yield on daisy chains





Daisy Chains

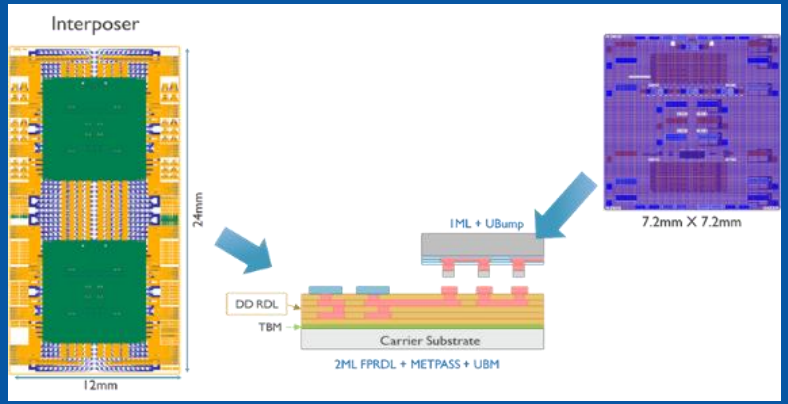


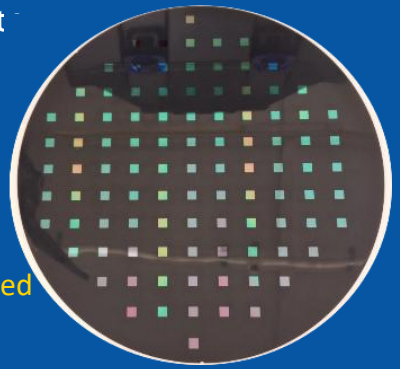


Co-funded by Chips JU

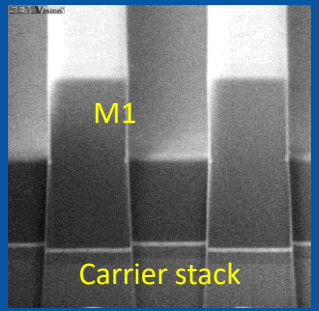
Fine pitch Redistribution Layer & chiplet assembly

- Fine pitch RDL
  - Enablement 1.3um metal width interconnect
- Chiplet assembly
  - Enablement 20um pitch die to RDL
- Towards platform flow for chiplet prototyping
- Solder balling & packaging on substrat
  Joint collaboration with Fraunhofer

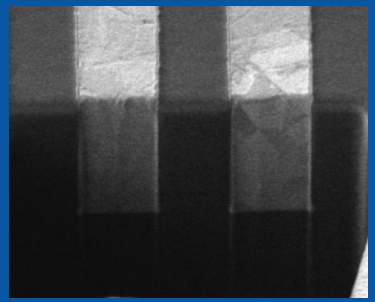




Reconstructed wafer



1.3 µm L/S lithography

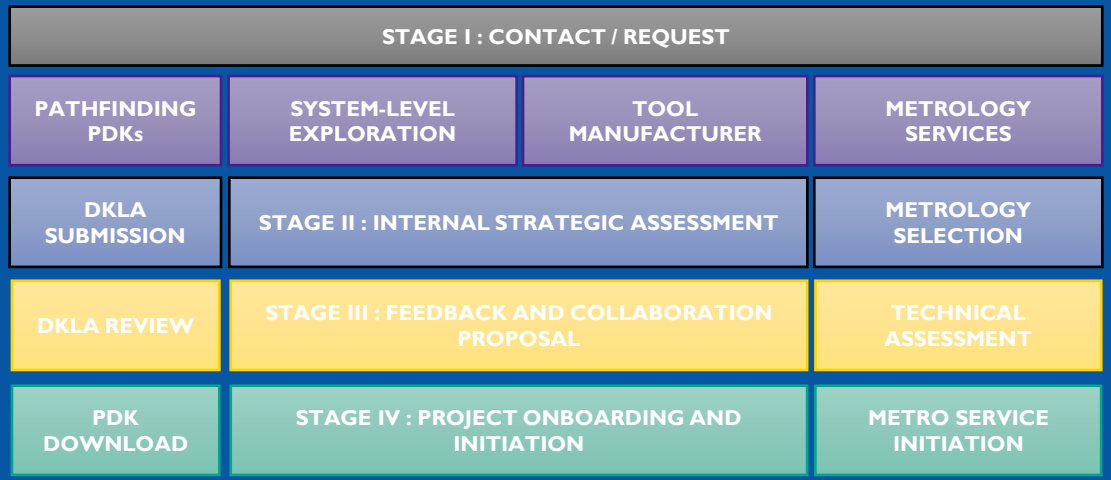


1.3 µm L/S after CMP

The NanoIC Access Process

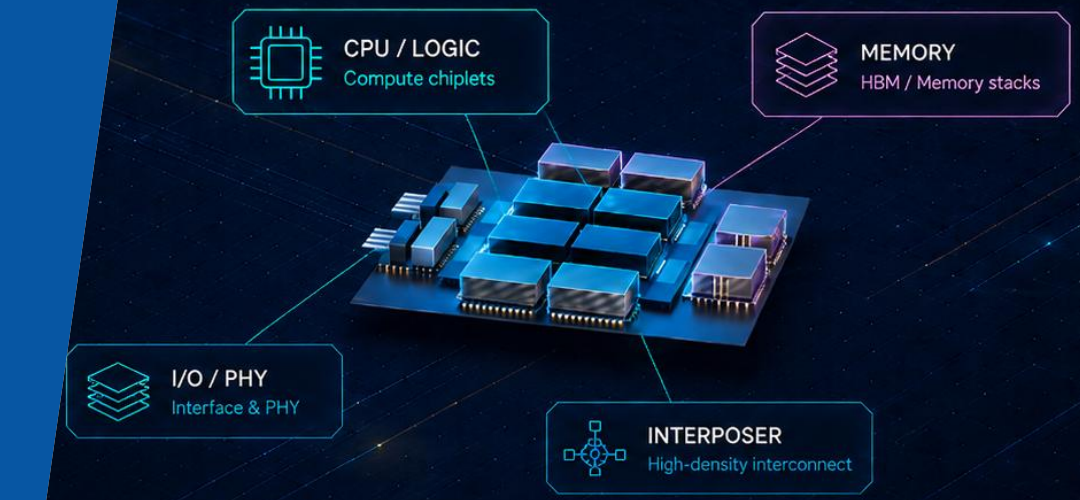


The NanoIC Access Process



- The NanoIC pilot line Pathfinding PDKs are accessible via the NanoIC webpage and the Europractice portal
- System Exploration PDKs will be available at a later stage
- Access flow for tool manufacturer is already active – several active potential leads
- Metrology services accessible @all project consortium sites

Pathfinding PDKs



NanoIC Pathfinding PDKs

Explorative design environment for Advanced Logic, Embedded Memories and Advanced Interconnect

- The NanoIC project provides a comprehensive PDK environment for
  - **designing,**
  - **experimenting** with, and
  - testing **innovative IC solutions** on advanced nodes.

- The PDKs are **continuously benchmarked**

  with physical devices (fabricated in imec's cleanrooms),

  for maximum adherence to **realistic electrical behavior** of devices.

- Almost all NanoIC technologies currently available as Pathfinding PDKs
  - Advanced Logic : N2 and A14
  - Novel Memories : EDRAM (SOT MRAM upcoming)
  - Advanced Interconnect : D2W and RDL (Interposer upcoming)

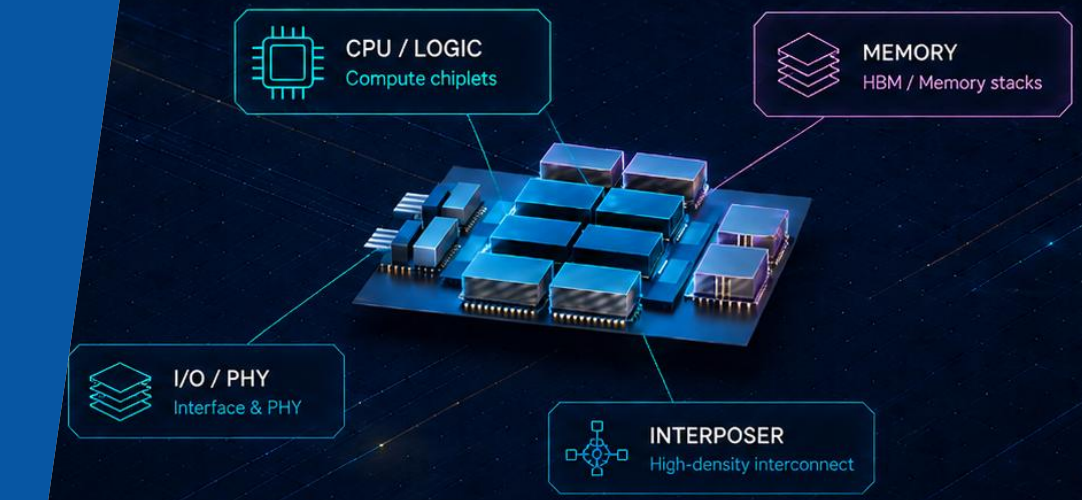
Free access

- **All PDKs require the signature of a standard Design Kit License Agreement : the Access will be automatically granted to entities headquartered in countries participating to Horizon+Digital programmes**

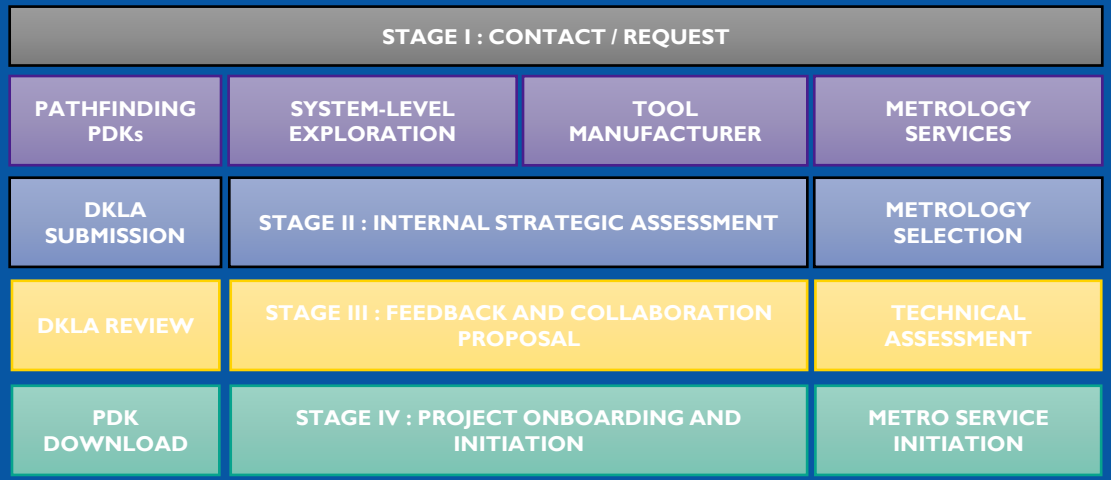
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Tool Manufacturer Access



The NanoIC Access Process for tool manufacturers

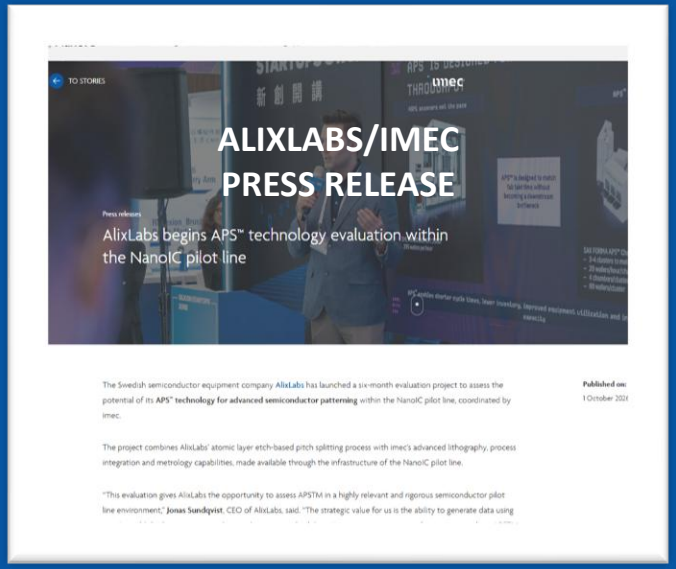


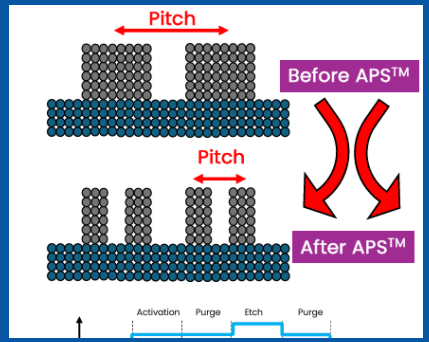
- Access for tool manufacturers enabled during 2025
  - More than 20 initial leads
  - 1 landed
  - 4 in the pipeline

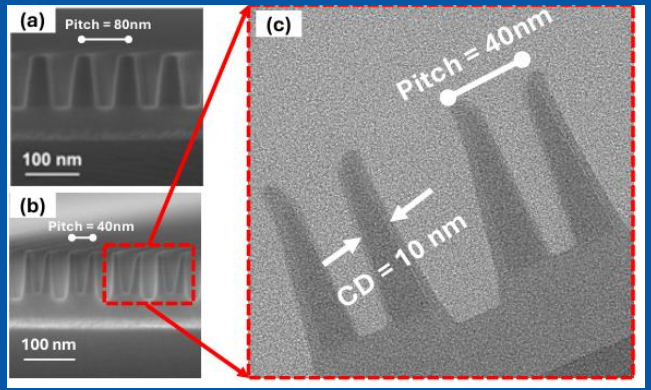
Alixlabs – NanoIC

Fin Patterning via single pitch splitting approach

- During Sept 2026 the NanoIC PL and Alixlabs signed an Evaluation Agreement focused on Pitch Splitting etch technology validation.



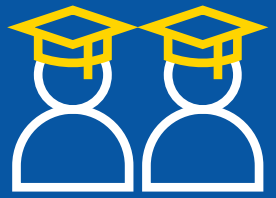




Training and Workforce Development



To build a skilled European semiconductor workforce, the NanoIC pilot line offers:



Opportunities for **PhD** students and **interns**



PDK workshops



Seasonal Schools



Expert courses

OPPORTUNITIES FOR PHD STUDENTS AND INTERNS

nanoic-project.eu/en/student-opportunities



imec

imec research internships

- hands-on experience in the world's leading research center
- BSc | MSc | PhD
- 3 to 18 months
- Latest internship call : May-June 2026

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Tyndall National Institute

Summer Fellowships

- an immersive, hands-on research experience with renowned experts in cutting-edge fields
- 3 months research project + workshop series
- Applications for summer 2027 edition open December/January

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- opportunity to work on groundbreaking research that shapes the future
- joining a vibrant community of > 800 PhD students from 40+ countries
- Upcoming window for PhD applications:

  June 22nd - July 8th, 2026

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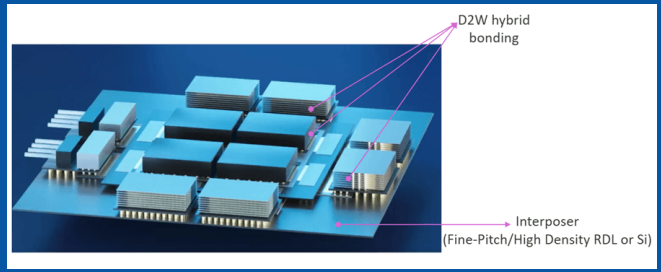
imec Student Excellence Day

- opportunity to explore the cutting edge of chip technology from research to real-world applications
- for: 3rd year BSc, MSc, PhD students in a STEM field
- 2x / year (spring & winter)
- Save the date: November 25th, 2026

Interposer, RDL & D2W Pathfinding PDK training

REGISTER HERE

- Advanced PDK workshop: Interposer, fine-pitch RDL & D2W hybrid bonding 7-8 December 2026
- 2 days with hands-on workshop
- Audience: students, academics, and professionals
- Location: imec, Leuven, Belgium



3D stack representation with D2W hybrid bonding and fine-pitch RDL interposer

NanoIC European Winter School on Patterning

- Technical presentations on: CMOS processing, lithography, patterning, photoresists, mask technology, ALE, ASD, metrology, …
- 2 days | 138 participants





NanoIC Spring School on Advanced CMOS

- Technical presentations on: process integration, materials science, characterization, test structures and vehicles, and patterning, …
- Following imec Students Excellence Day to promote student participation
- 2 days | 144 participants

Save the date:
- NanoIC European Winter School 2026
- November 26th – 27th, 2026

Nanosheet (N2,A14) Pathfinding PDK trainings

- Advanced PDK Workshop: N2-A14 Nanosheet Pathfinding & Applications
- Theoretical foundations of the N2 and A14 technologies, practical design strategies, and implementation in digital design flow
- 2 days: lectures + hands-on with the N2 and the A14 Nanosheet Pathfinding-PDKs (P-PDKs)
- Audience: students, academics, and professionals
- Location: imec, Leuven, Belgium





NanoIC

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Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or Chips Joint Undertaking. Neither the European Union nor the granting authority can be held responsible for them.

Coordinated by imec

Co-funded by

Chips JU

Supported by

Vlaamse overheid

Pilot line project partners

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Fraunhofer MIKROELEKTRONIK

cea leti

VTT

Politehnica Bucharest

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