EuroCDP
EU Chips Design Platform

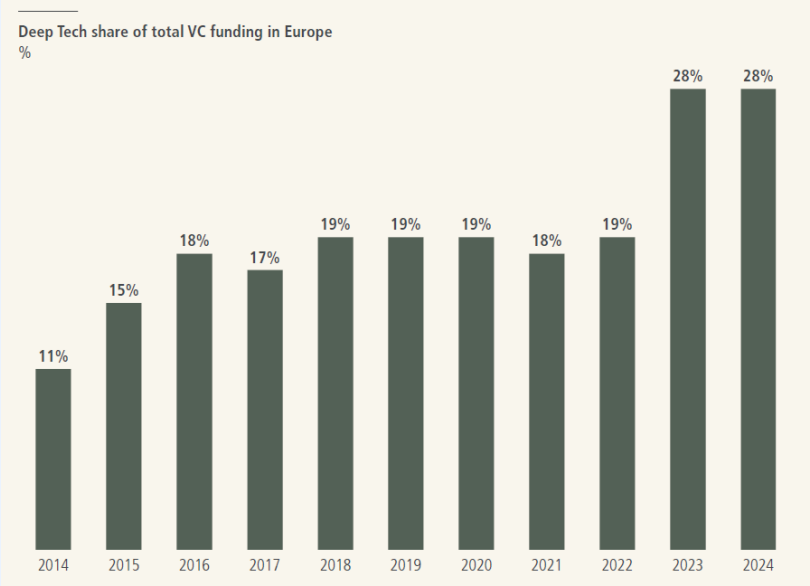
European Chips Design Platform

Removing Barriers to Next-Generation Chip Design

Denis Villers

Semiconductors ➔ Global economic growth

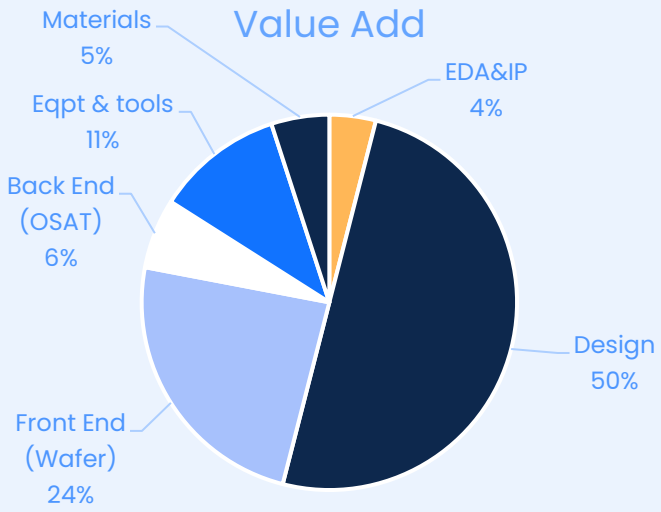
- Essential infrastructure for AI, HPC, automotive, mobile, robotics
- Outperforming sector in growth and market cap
- Capital-attractive & resilient vs. traditional tech cycles



Semiconductors are no longer a niche industry — they are macro-economic infrastructure

IC design

- Highest value-added layer
  - ~50% of total GVA
- Upstream leverage
  - Design demands drive manufacturing capacity
- Primary source of differentiation and innovation
  - AI accelerators, domain-specific chips



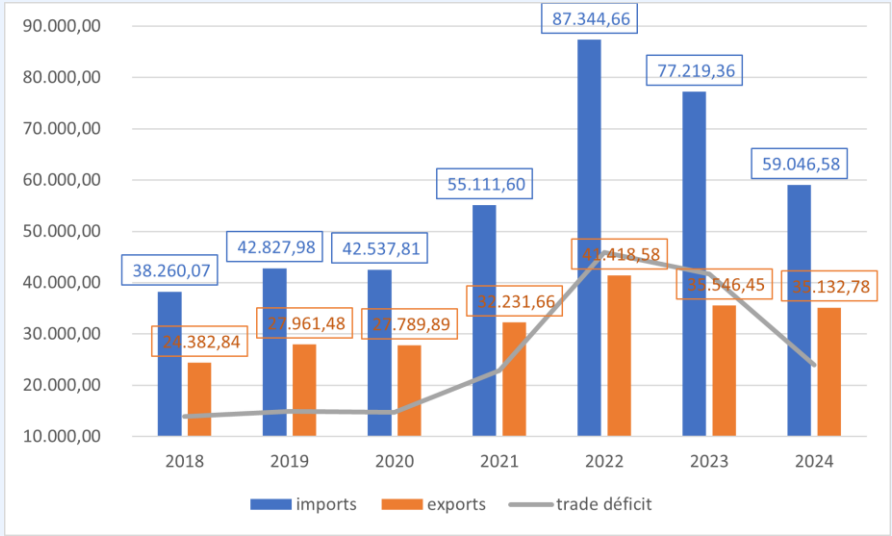
Source: BCG analysis using data (Capital Iqand Gartner)

The highest value in the semiconductor value chain

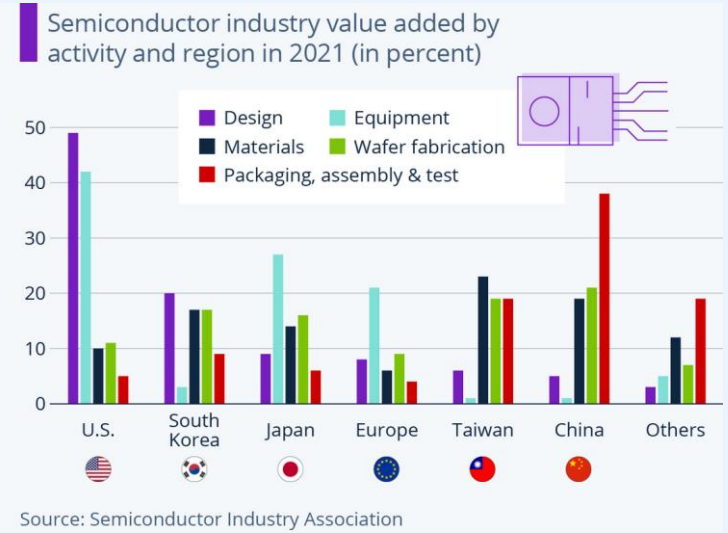
In Europe

- Strength:
  - Strong market growth (+32% since 2021)
  - World-class leaders (ASML, ST, Infineon, NXP)
  - Excellence in pre-competitive research
- Structural gaps:
  - Highly concentrated market (~65% controlled by 4 players)
  - ~95% of companies are SMEs, but under-supported
  - Fabless IC design <10% market share → untapped growth potential

Fabless **SMEs are essential** for EU resilience and innovation.



The semiconductor market is shifting from global optimization to regional value chains



Structural barriers prevent European fabless innovation from scaling

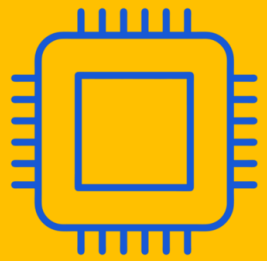
- Cost & complexity
  - IC development costs are skyrocketing
  - Advanced nodes require EDA, IP, tape-out access beyond SME reach
- Financing mismatch
  - Limited patient capital and fragmented funding instruments
  - Typical IC startup: €150M+ and 8–10 years to exit
- Innovation gaps (“death valleys”)
  - Lab → Prototype
  - Prototype → Industrial scale

These barriers cannot be solved individually

They require to act globally

EuroCDP objectives

Reduce design technical barriers



Overcome complexity of designing chips and fast track prototyping

Reduce design cost barriers



Access affordable EDA tools, IP, design services to lower entry costs

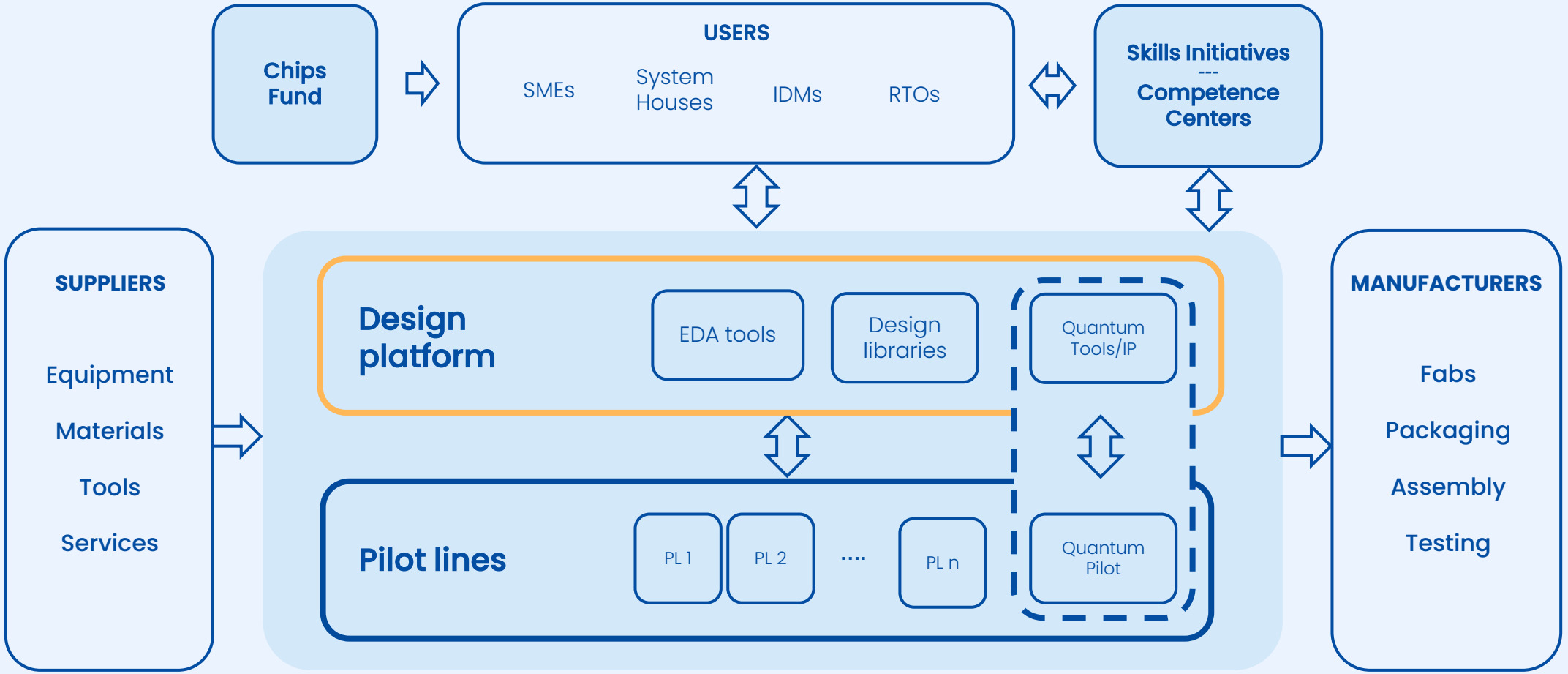
Support Ventures development



Support SUs to face Lab-to-Prototype and Prototype-to-Scale death valleys

An integrated platform offering all essential services in one place

EuroCDP at the heart of EC strategy to reinforce EU Chip market share



PCT consortium

Consortium

- 12 partners
- 11 state members
- 8 RTOs, 4 universities
- 5 pilot lines representatives
- Europractice representative
- IC, PIC, Quantum, Open source
- 81 support letters



EuroCDP Value Proposition for EU Fabless

Chip Design Support

- **Technical training** access
- Cloud-based **Computing & Storage capacities**
- Open source **IP & EDA**
- **Sandbox** for exploration

SME Financial Support

- Users' project **grants** for
  - IP & EDA
  - Infrastructure
  - DET services (fabrication)
- **Negotiated** Commercial EDA & IP licenses

Entrepreneurship Support

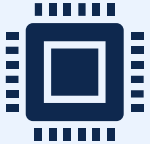
- **Mentoring**
- **Incubation program** to enable start-ups ideas to take root and grow
- **Accelerator program** to boost start-ups to scale

Chip Design Services



Fabless use-case

CHIP DESIGN JOURNEY



Industrial solution

central cloud

EDA framework | IPs | Manufacturing | Tests | Debug

Pathfinding
- Ideation
- Training
- Sandbox

EuroCDP + CCC

Design
- Design flow
- Expertise
- IP sourcing

Prototyping
- MPW shuttles
- Assembly
- Test

Ramp-up
- Private shuttles
- Qualification
- Supply Chain

EuroCDP

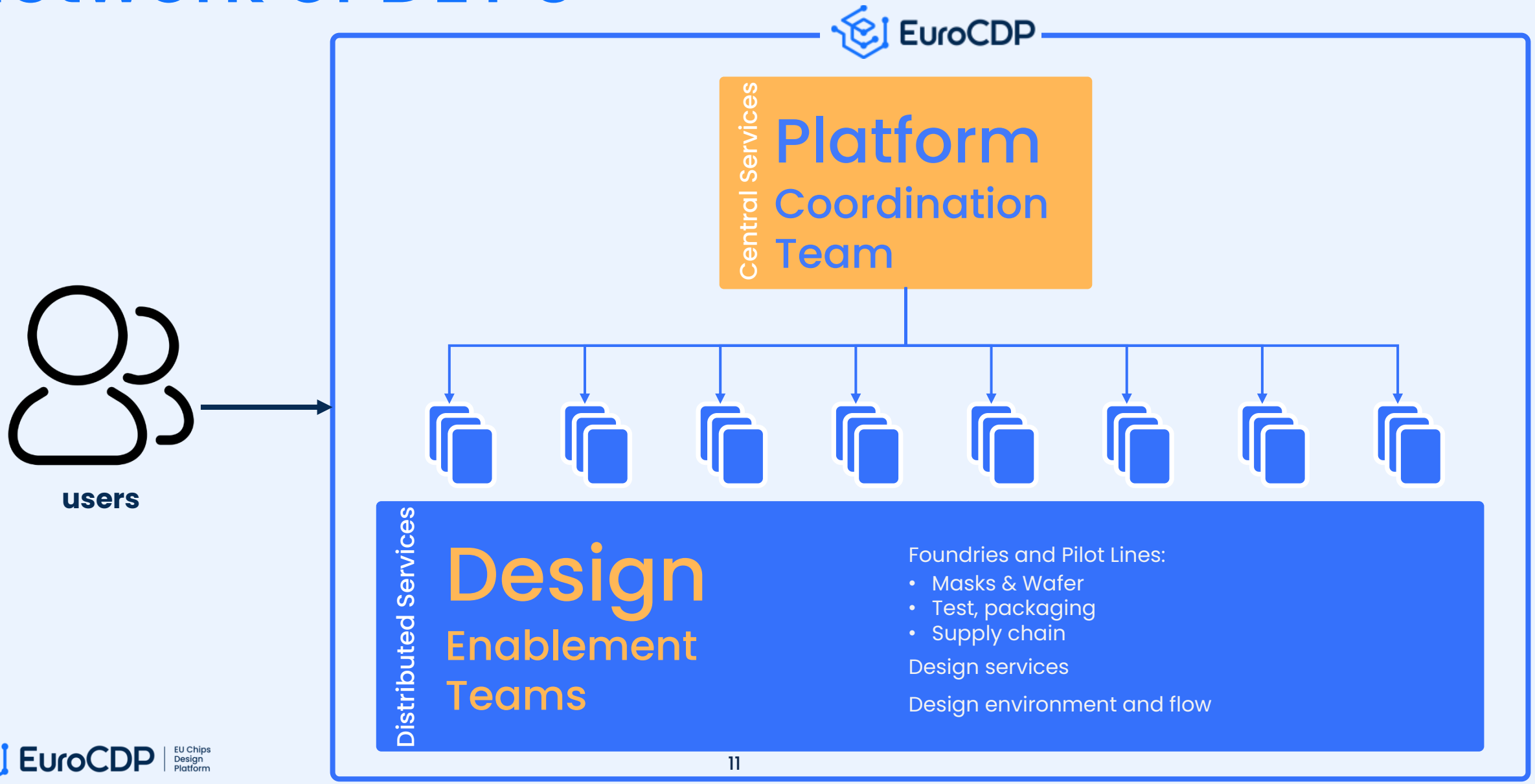
Production
- Scalability
- Operational support
- Secure Supply Chain

DETs

incubation — acceleration

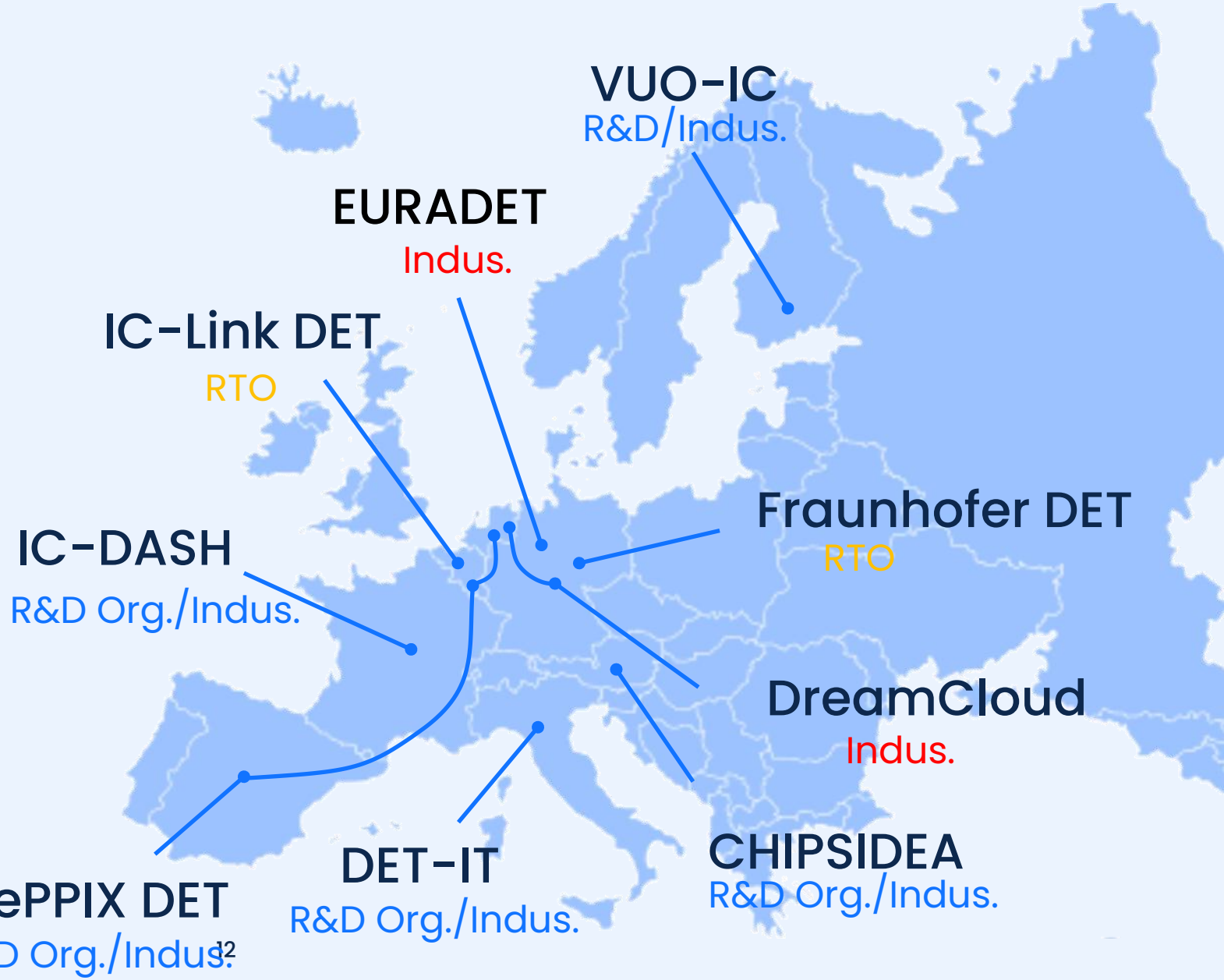
orientation programme | startup programmes | product and volume

Network of DET's



DET Overview

- 9 DETs over 8 Member States
  - 5 Consortia
  - 4 Single entities (RTO or Industrial)
- Ecosystem:
  - Industrial, R&D organization (Acad./RTO)
  - 5 pilot lines
  - GF, ST, tsmc, xFab, Samsung, Intel
  - Suppliers & turnkey partners
- Technologies / Domains
  - Bulk, SOI, FinFet (down to 2nm)
  - GaN/GaS, SiC, SiGe
  - NVM, 3D integration, Photonic
  - RF, Analog, Mixed signal, Digital
  - From industry to Defense app.



EuroCDP | EU Chips Design Platform

User eligibility to EuroCDP advanced services

START-UPs



SMEs

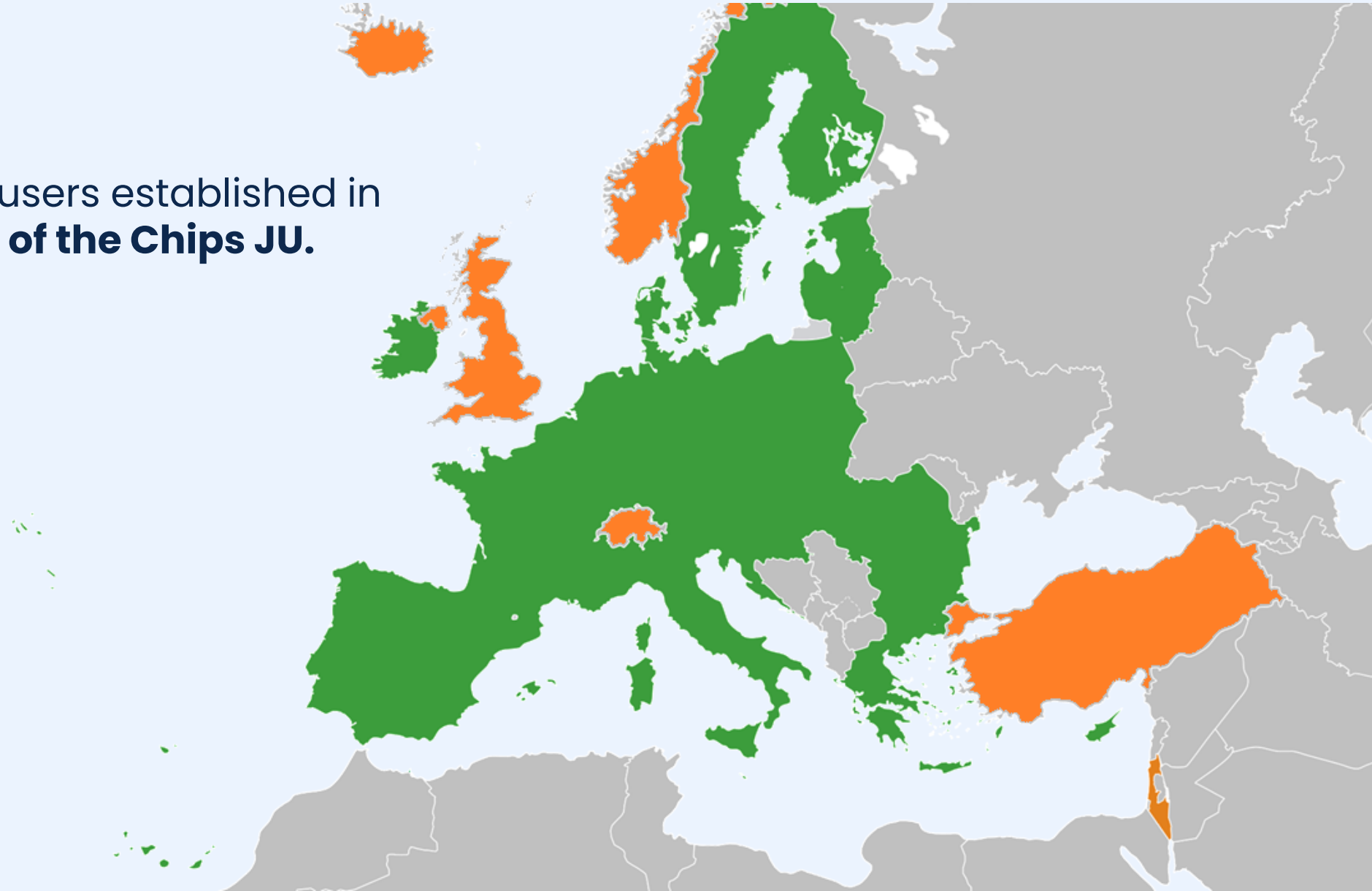


MID-CAPs

LARGE-CAPs

Access conditions

- **Access is limited** to users established in **Participating States of the Chips JU.**



EuroCDP | EU Chips Design Platform

Access conditions

- Entities established in a Participating State but **directly or indirectly controlled by a third country:**

  We can grant access if directly or indirectly controlled by an **OECD or Mercosur country**, upon two main criteria:

EU added value

Economic security



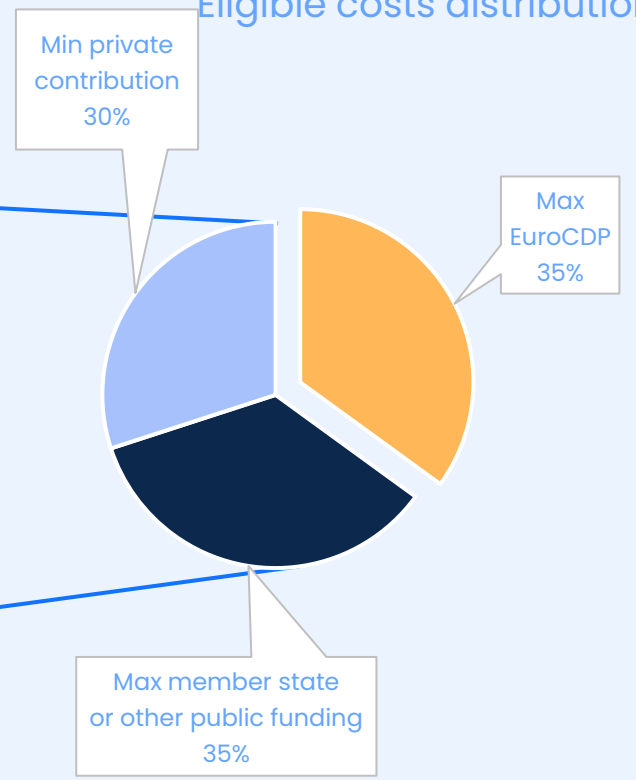
Eligible costs

SME Financial Support

Users' project **grants** for
- IP & EDA
- Infrastructure
- DET services (fabrication)

Negotiated Commercial EDA & IP licenses

Eligible costs distribution



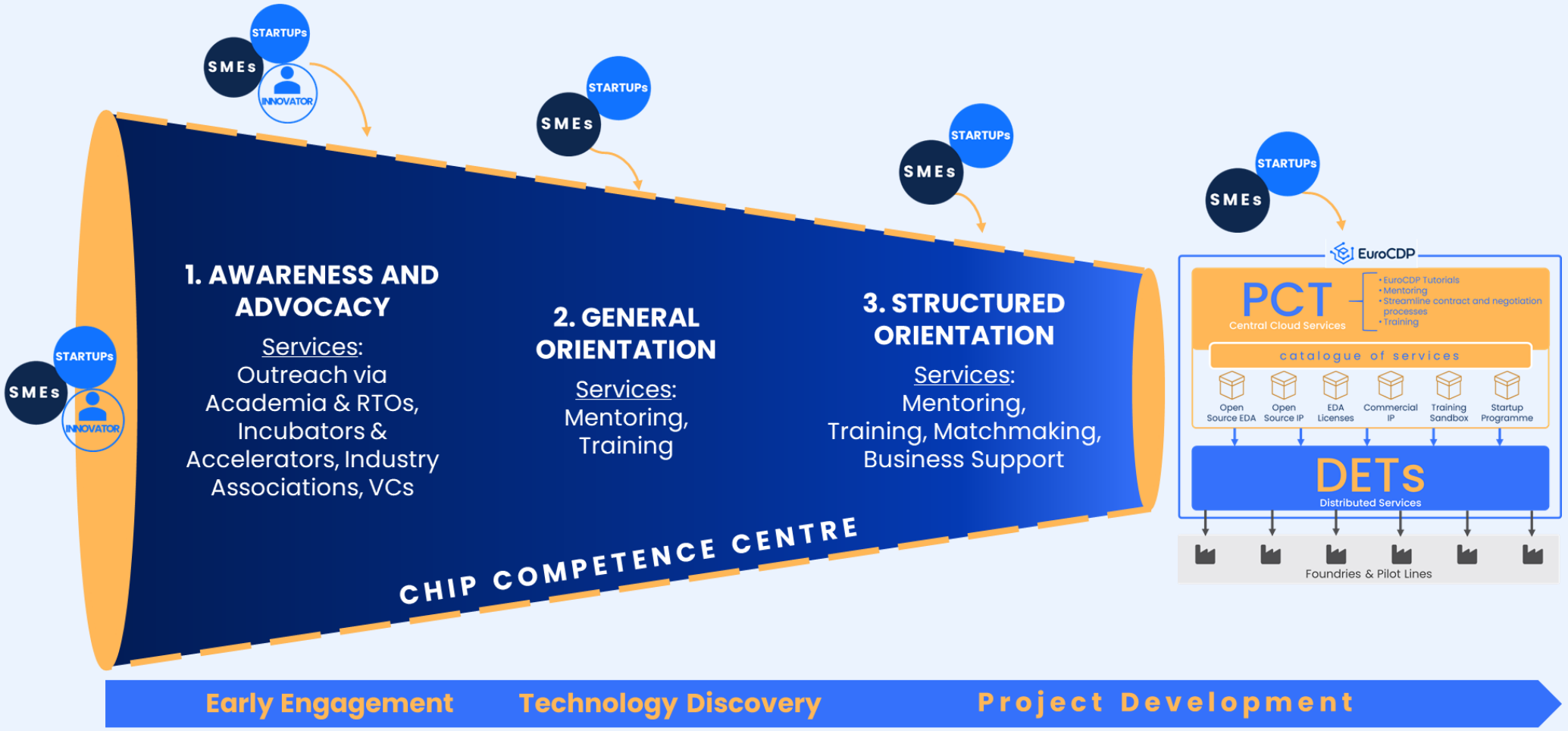
By company:

Max LV1:	100 k EUR
Max LV2:	8 M EUR

Max L2 eligible costs:	22,8 M€
Max L2 EuroCDP contribution:	8 M€

Interaction with Chip Competence Centers

- Start-ups and SMEs funnel



Join the EuroCDP community!

From idea to chip — faster, together.

EuroCDP

EU Chips Design Platform

www.eurocdp.eu

This initiative is supported by Chips JU and the European Commission.

EUROPEAN PARTNERSHIP

EuroCDP
EU Chips Design Platform

Your go-to platform in Chip Design.

Thank you!

This initiative is supported by Chips JU and the European Commission.

EUROPEAN PARTNERSHIP