ROADSHOW

APECS

Forschungsfabrik Mikroelektronik Deutschland

A cooperation of Fraunhofer MIKROELEKTRONIK

Forschungsfabrik Mikroelektronik Deutschland

Research Fab Microelectronics Germany (FMD)

A cooperation of 13 Fraunhofer institutes and the Leibniz institutes FBH and IHP

Profile and Specifics

Research Fab Microelectronics Germany (FMD)

13 Fraunhofer and
2 Leibniz institutes

> **5,400*** employees,
including > **2,900*** scientists

First patent applications: **191**
Active patent families: **2986**

19,500 m²
cleanroom space
ISO9001 certification
1 MES over 10 institutes

> **2,200 tools/equipment**
in **13 cleanrooms**

€ 2.2 bn Assets/Investment

€ 673 m Budget/a

€ 272 m Industry projects

Applied research with solid foundation in academic research/education and technology transfer as a mission

Research on heterogeneous systems integration and advanced packaging on EU level for technological sovereignty within the EU Chips Act

Special commitment to green ICT, quantum and neuromorphic computing, chip design, heterogeneous systems integration and trusted electronics

Project oriented funding model with small share of basic funding

Strong link to applications / industry

Distributed structure as group of institutes

Young talent development

*Number of employees incl. AISEC and IMWS. Given figures relate to 2023.

Research Fab Microelectronics Germany (FMD)

Cooperation between 13 Fraunhofer and 2 Leibniz institutes

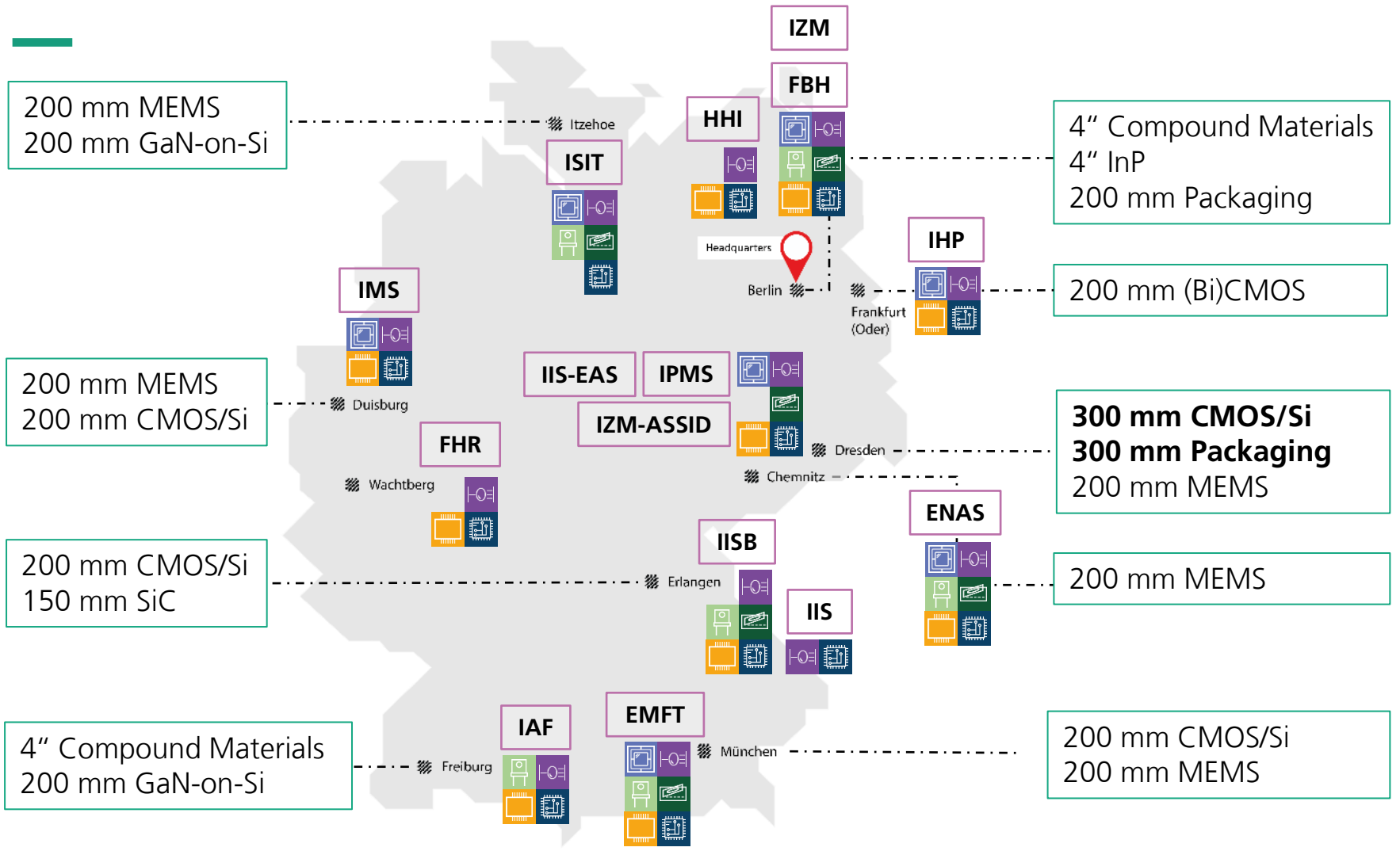
Fraunhofer Institute for

- Applied Solid State Physics **IAF**
- Applied and Integrated Security **AISEC**
- Electronic Nano Systems **ENAS**
- High Frequency Physics and Radar Techniques **FHR**
- Integrated Circuits **IIS**
- Integrated Systems and Device Technology **IISB**
- Microelectronics Circuits and Systems **IMS**
- Microstructure of Materials and Systems **IMWS**
- Electronic Microsystems and Solid State Technologies **EMFT**
- Telecommunications, Heinrich-Hertz-Institut **HHI**
- Photonic Microsystems **IPMS**
- Silicon Technology **ISIT**
- Reliability and Microintegration **IZM**

Leibniz Institutes

- Ferdinand-Braun-Institut gGmbH, Leibniz-Institut fuer Hoechstfrequenztechnik **FBH**
- Leibniz-Institute for High Performance Microelectronics **IHP GmbH**

FMD Cleanrooms and Technology Platforms all over Germany



200 mm MEMS
200 mm GaN-on-Si

4“ Compound Materials
4“ InP
200 mm Packaging

200 mm (Bi)CMOS

200 mm MEMS
200 mm CMOS/Si

300 mm CMOS/Si
300 mm Packaging
200 mm MEMS

200 mm CMOS/Si
150 mm SiC

200 mm MEMS

4“ Compound Materials
200 mm GaN-on-Si

200 mm CMOS/Si
200 mm MEMS

FMD Technology Platforms

- Extended CMOS
- Optoelectronic Systems
- Power Electronics
- MEMS Actuators
- Microwave and Terahertz
- Sensor Systems

Technology Platforms

Research Fab Microelectronics Germany

1 Sensor Systems
Sensor design, fabrication, integration, characterization, and testing within systems

2 Microwave and Terahertz
Cutting-edge devices and circuits for frequencies up to and including the THz range

3 MEMS Actuators
Design and fabrication, as well as characterization, testing and system integration of MEMS actuators

4 Extended CMOS
Design, fabrication and system integration of CMOS circuits

5 Power Electronics
Design and fabrication of power electronic devices, including integration in modules and systems

6 Optoelectronic Systems
Fully integrated optoelectronic systems for image acquisition and processing, and communication up to Tbit/s speed

7 Chip- und Chiplet-Design
Design of computer chips in which either a single integrated circuit (chip) is developed or several small, independent chips (chiplets) are integrated into a system in order to optimise performance, efficiency and functionality

8 Multi Project Technologies (MPT)
Product prototyping / IP verification / Design libraries / Device characterization / Low volume manufacturing / "Proof of concept"/ Experiments with new circuits / First Silicon verification

Peak Performance in Heterogeneous Integration

Pilot Line for Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems (APECS)

Research Fab Microelectronics Germany (FMD)

Coordinated by

Fraunhofer

Implemented by

Forschungsfabrik Mikroelektronik Deutschland

Pilot Line Project Partners

Fraunhofer MIKROELEKTRONIK
Leibniz Ferdinand Braun Institut
ihp
TU Graz
VTT
imec
cea leti
FORTH FOUNDATION FOR RESEARCH AND TECHNOLOGY - HELLAS
CNM CSIC
INL INTERNATIONAL IBERIAN NANOTECHNOLOGY LABORATORY

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Chips JU

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Ministry of Economic Affairs and Employment of Finland
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Flanders State of the Art
HELLENIC REPUBLIC MINISTRY OF DEVELOPMENT
Federal Ministry Republic of Austria Climate Action, Environment, Energy, Mobility, Innovation and Technology
MINISTERIO PARA LA TRANSFORMACIÓN DIGITAL Y DE LA FUNCIÓN PÚBLICA
BUSINESS FINLAND
CCDR NORTE
anr agence nationale de la recherche
FFG Promoting Innovation.

APECS is co-funded by the Chips Joint Undertaking and national funding authorities of Austria, Belgium, Finland, France, Germany, Greece, Portugal, Spain, through the Chips for Europe Initiative.

APECS Work Flow

Connecting design, technology and testing

Design Flows

System Design

- STCO Design for 2.5D / 3D
- STCO Design for QMI
- Foundational Chiplets

STCO = System Technology Co-Optimization
QMI = Quasi-monolithic integration

Interface Processing: Chiplet integration

Hetero-integration into (quasi-)monolithic integration (QMI)

Chiplet Integration platform (2.5D and 3D)

Front End Integration:

- RF Integration
- Photonic Integration
- QMI-Systems

HF = High frequency
QMI = Quasi-monolithic integration

Back End Integration:

- Advanced Packaging
- Functional Integration
- Functional Interposer

Analysis & Metrology

Character., Test & Reliability

- Characterization
- Reliability
- Test

Demos & Application Solutions

Access via One-Stop-Shop

Technological Background

Complexity of Advanced Heterogeneous System Integration

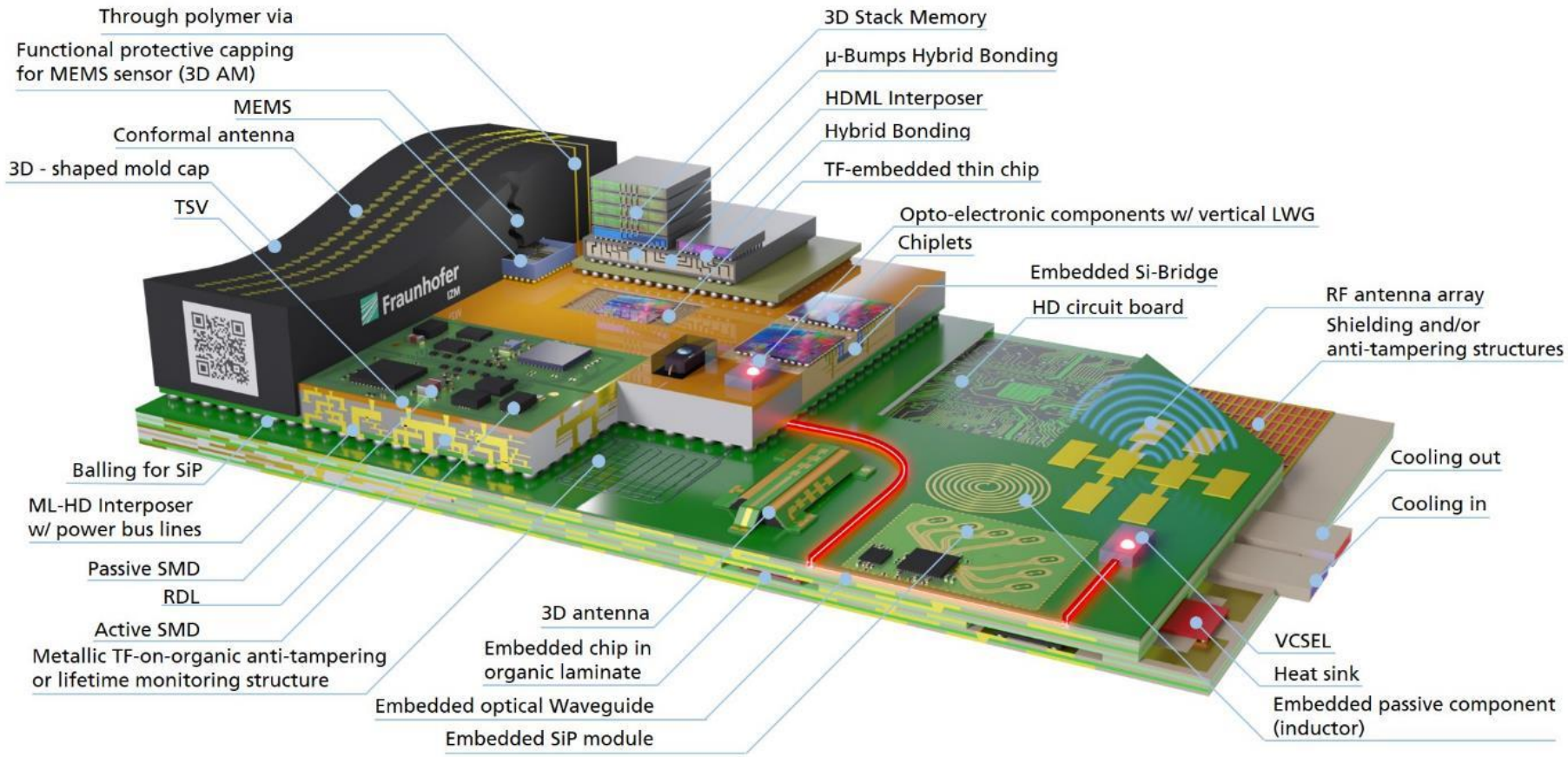


Image: Illustration of possibilities and the complexity of advanced heterogeneous system integration and advanced packaging. © Fraunhofer IZM

Demonstrators of the APECS pilot line

Demo 3: Photonic Integration

Target

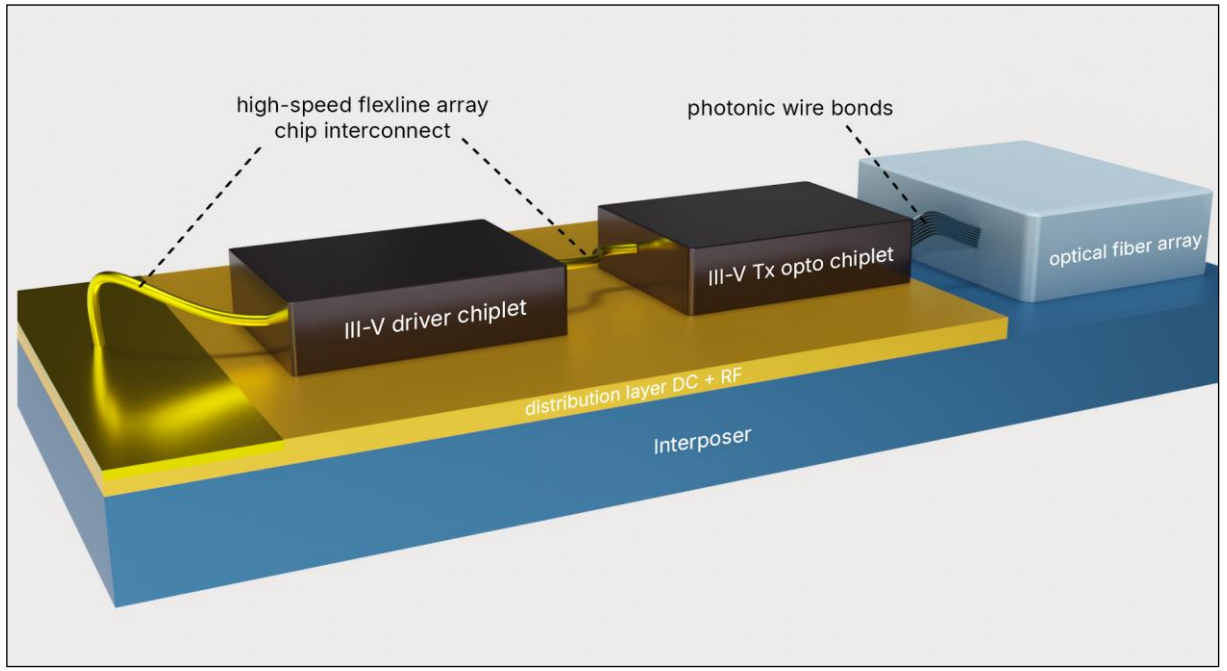
- Novel back-end-of-line interface technologies for photonic chips based on InP
- Ultra-high speed InP transmitter chiplets for optical interconnects

Innovations

- High speed InP chiplets as arrays allowing for e.g. 800Gb/s data transmission
- Integrated electrical and optical interfaces between EML chiplet, driver chiplet, interposer chip and optical fiber connections

Impact

- Quasi-monolithic integration of InP chiplets with additional components
  such as waveguides, resonators, couplers and gratings



Thanks for Your Attention

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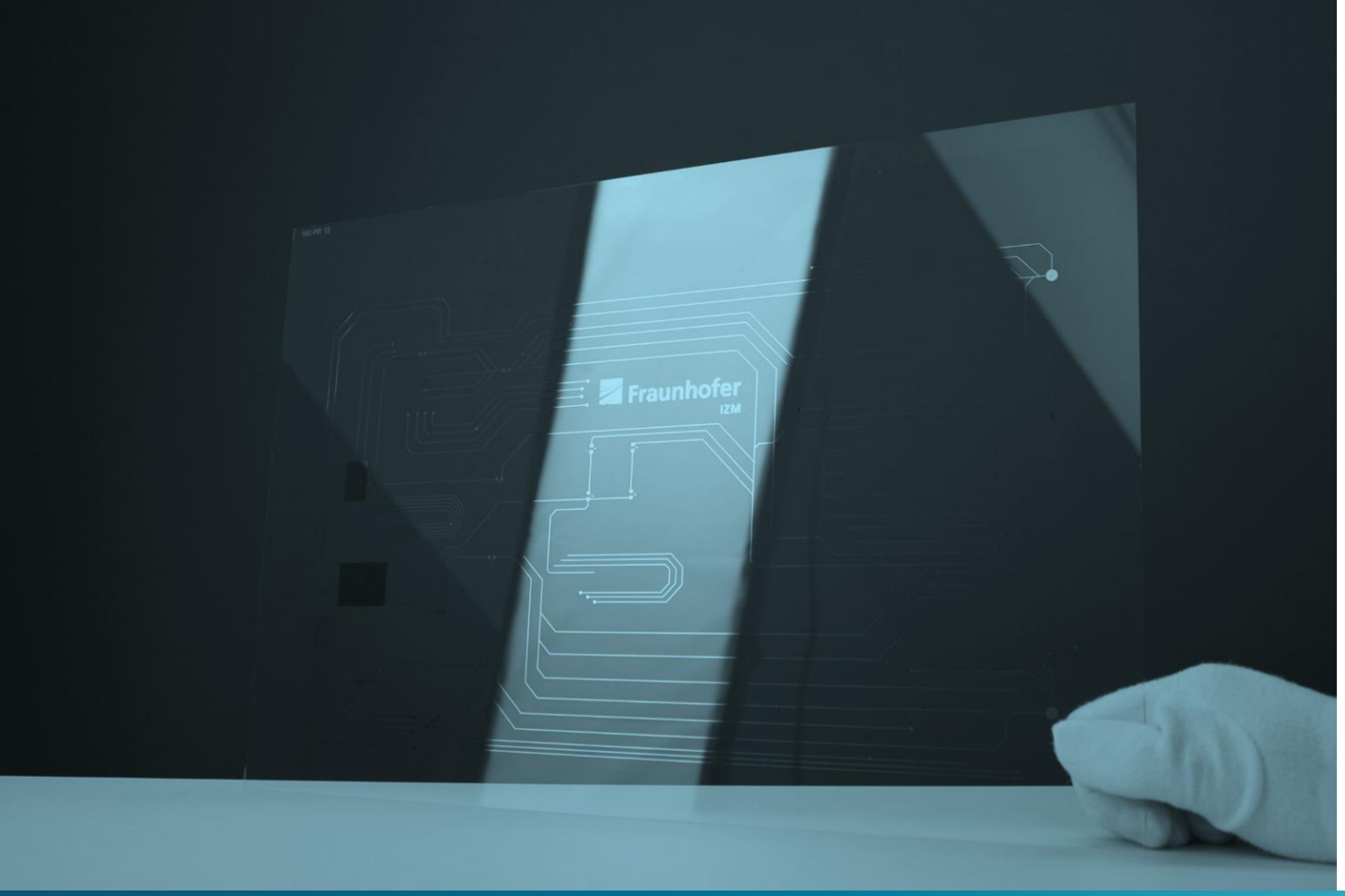


Fraunhofer
IZM

Fraunhofer Institute for Reliability
and Microintegration IZM

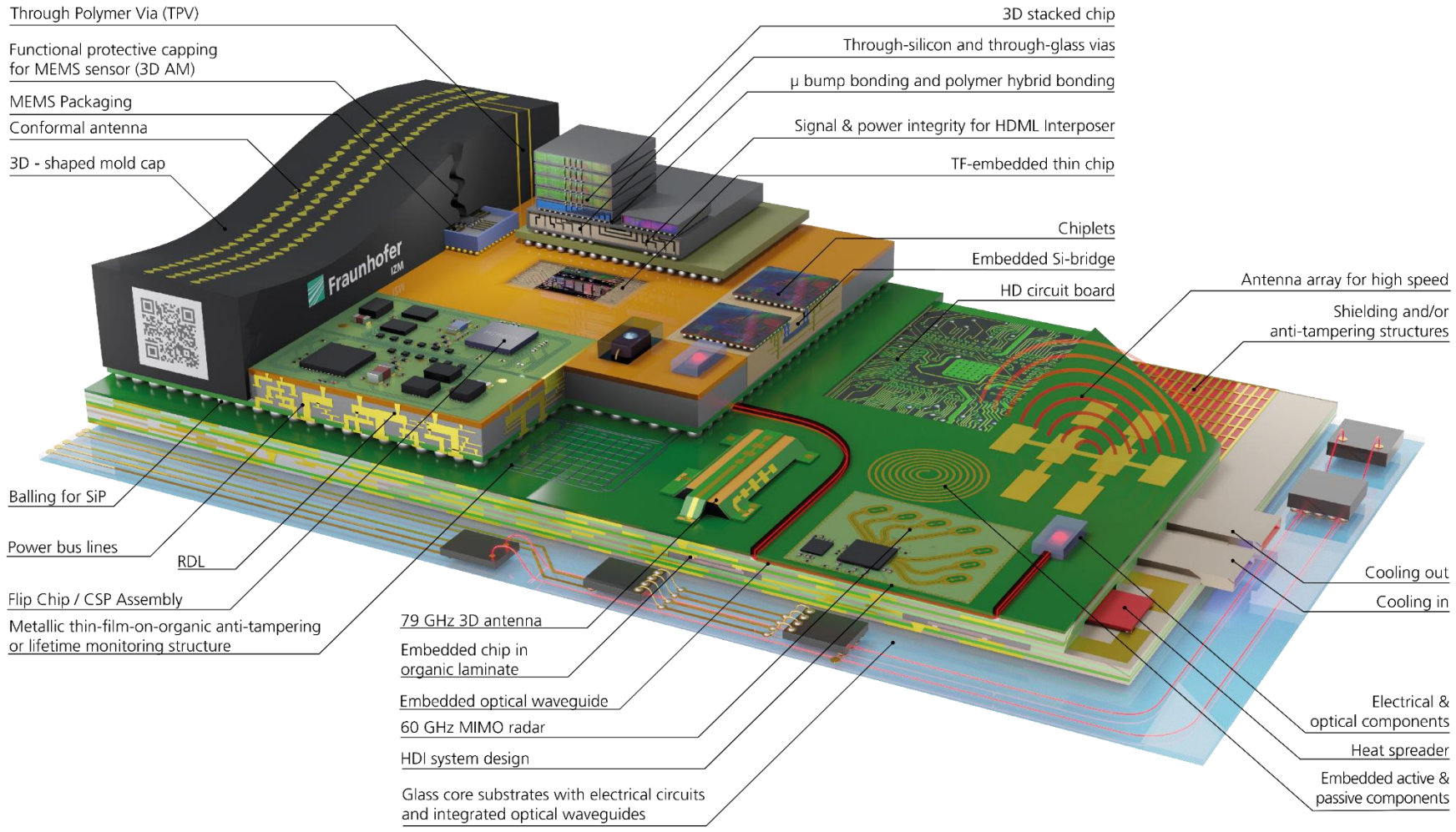
Fraunhofer IZM – Julian Schwietering

2025-12-10

APECS – Photonic Packaging at IZM

Hetero-Integration Technologies and Advanced Packaging

Bringing microelectronics into application



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Fraunhofer IZM

OIT – Optical Interconnection Technologies

The group includes three teams

Heads: Dr. Henning Schröder & Julian Schwietering Industrial Relations Manager: Dr. Gunnar Böttger

PSA

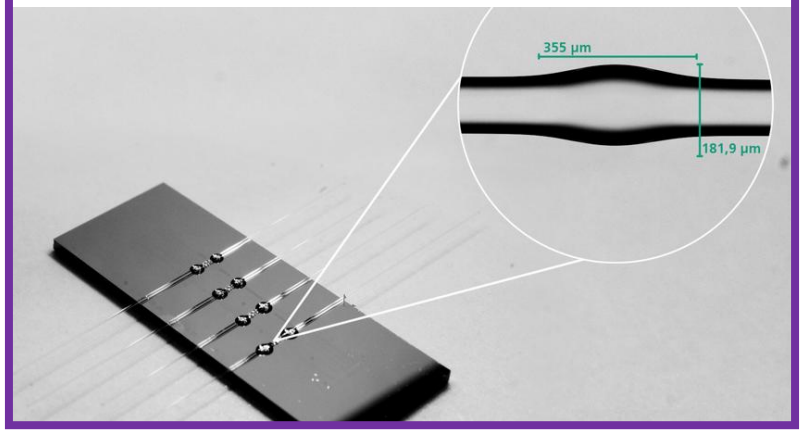
Photonic System Assembly

Dr. Wojciech Lewoczko-Adamczyk

FOIS

Fiber Optical Interconnects & Sensors

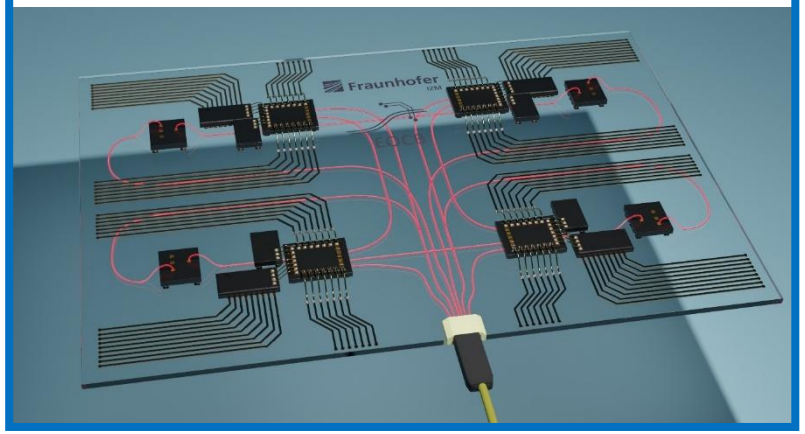
Dr. Wojciech Lewoczko-Adamczyk



EOCB

Electrical Optical Circuit Board

Julian Schwietering



In 2003 we named it:

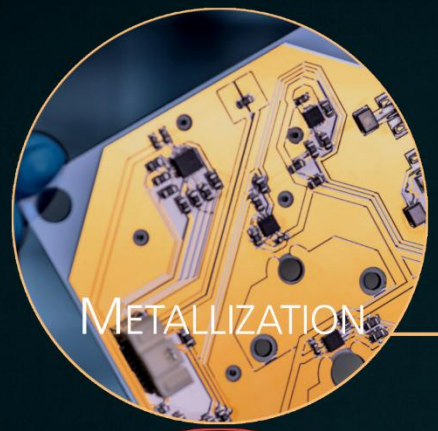
Electrical

-

Optical

-

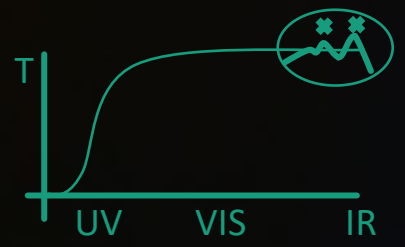
Circuit Board



How we should have named it

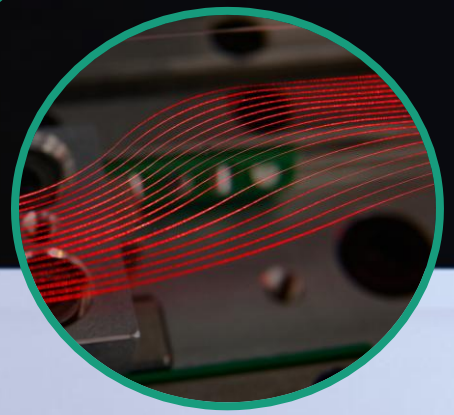
One important property of future photonic glass core substrates is:

Optical transparency



1310nm,
1550nm

Waveguides



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Fraunhofer IZM

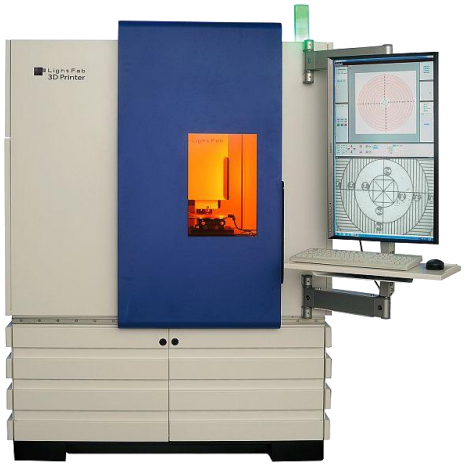
Optical Waveguides in Glass – Fabrication methods

Two methods are available at IZM to integrate waveguides into glass.

fs-Laser writing of waveguides

- direct writing of waveguides
- flexible 3D process

Machine at Fraunhofer IZM



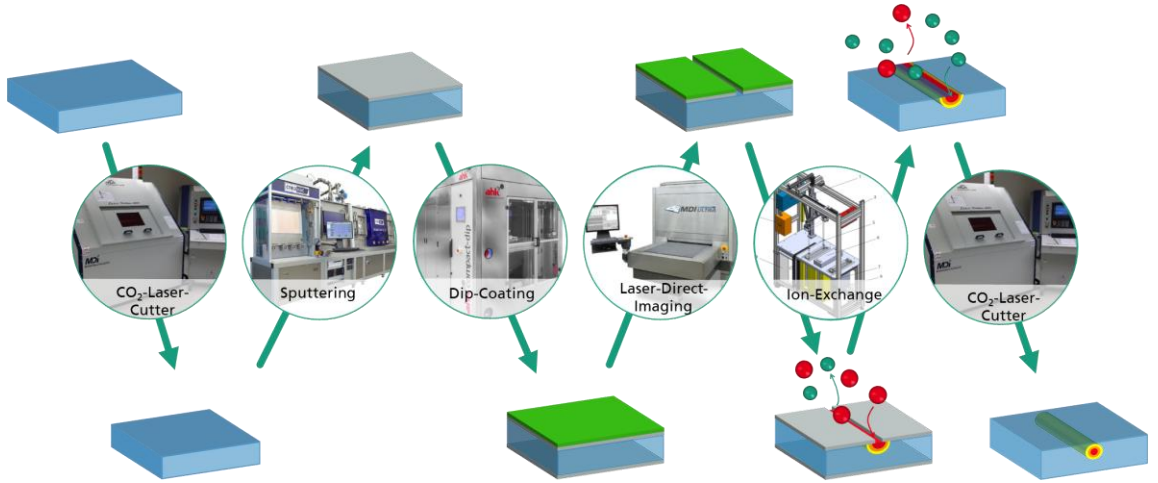
© LightFab

&

Ion exchange

- lithography based multi batch process to create waveguides
- much more robust process

Process chain at Fraunhofer IZM



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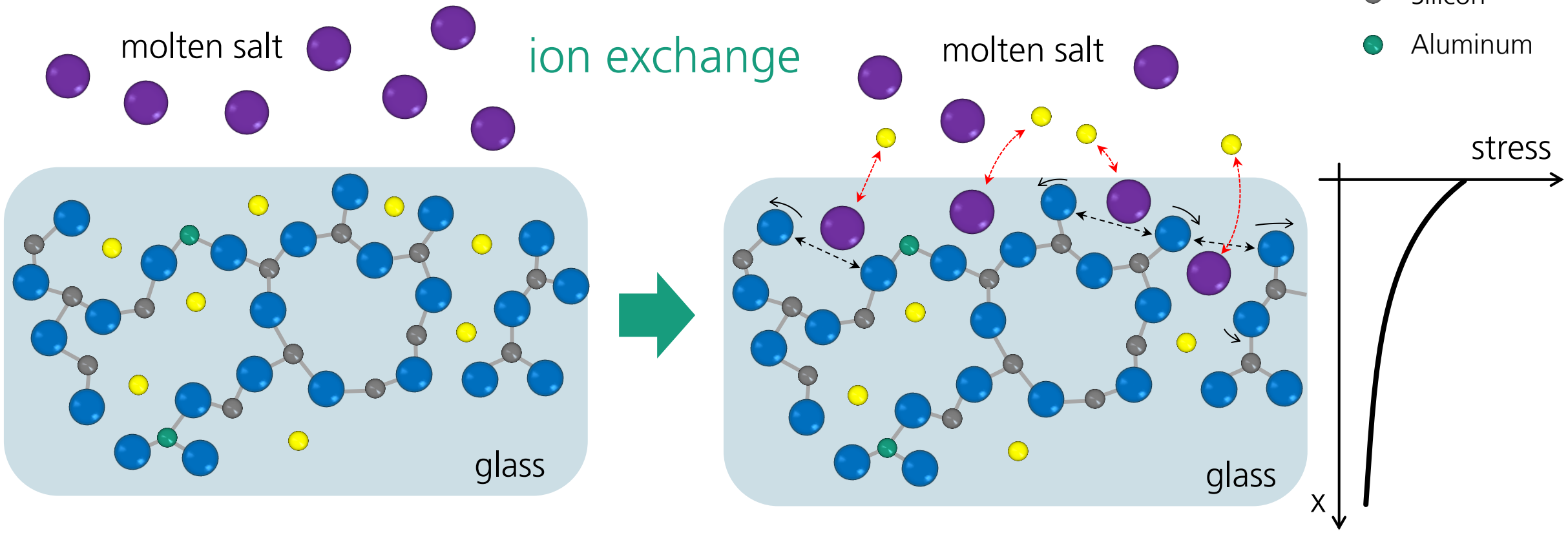
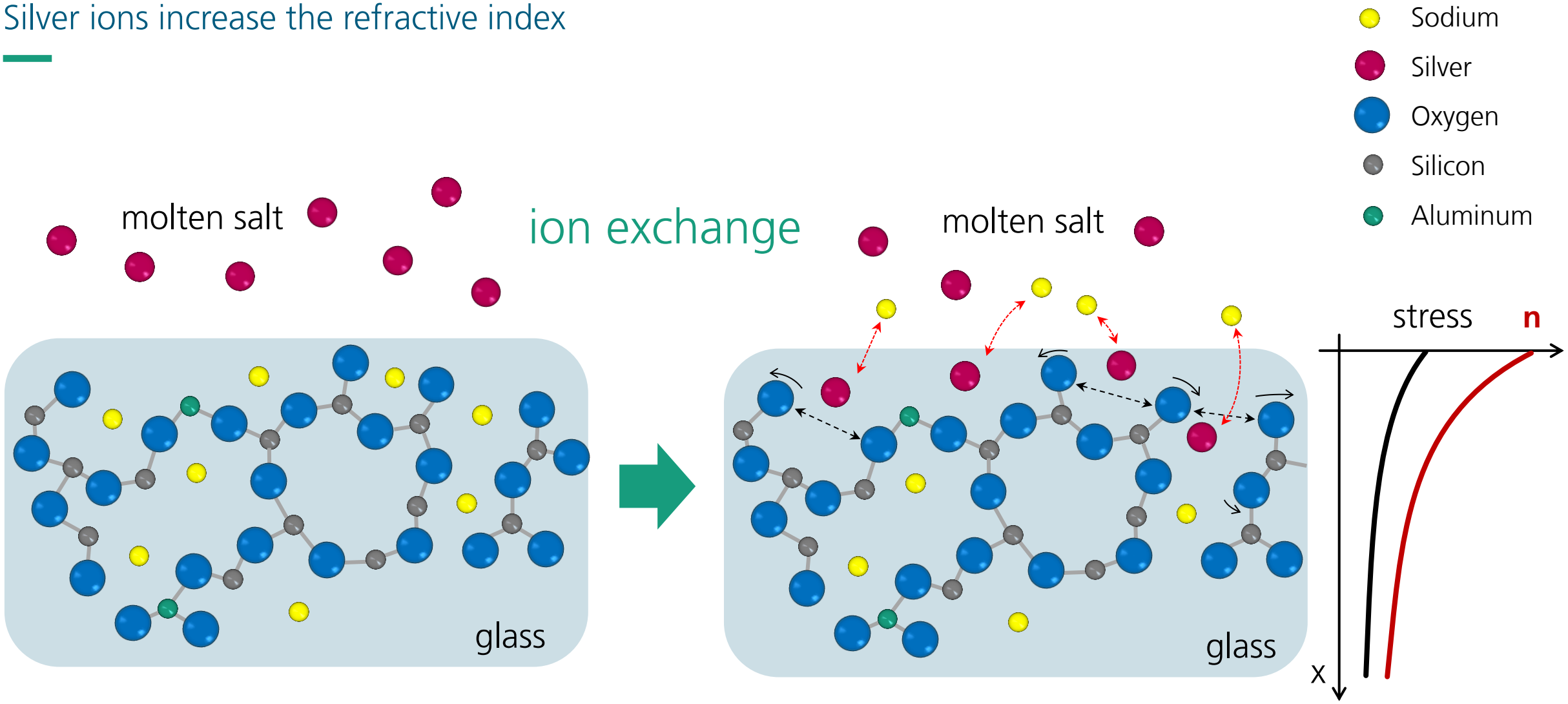
Optical Waveguides in Glass – Ion Exchange

The process for waveguide creation is equal to a process with a big impact on our everyday lives: chemical strengthening



Optical Waveguides in Glass – Ion Exchange

Silver ions increase the refractive index

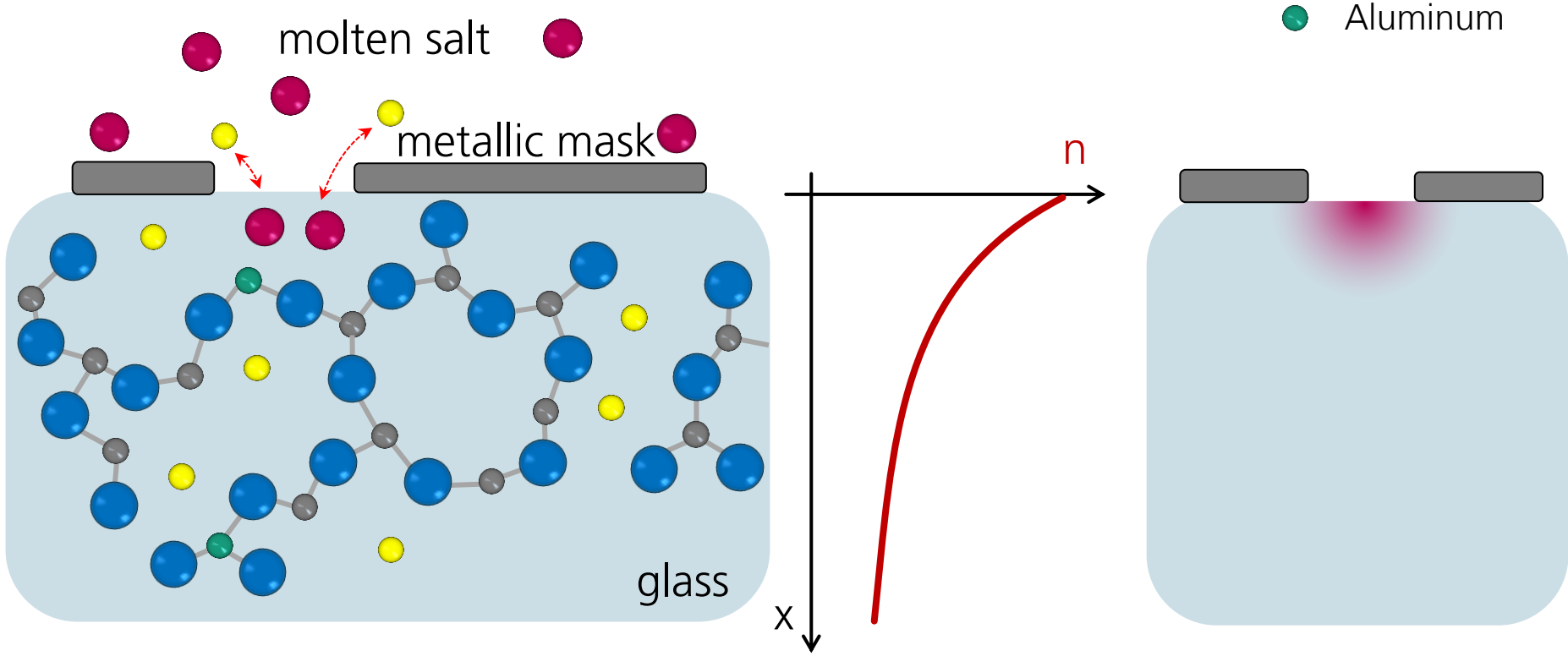


Optical Waveguides in Glass – Ion Exchange

The diffusion through a mask creates surface waveguides

Sodium
Silver
Oxygen
Silicon
Aluminum

1) Ion exchange



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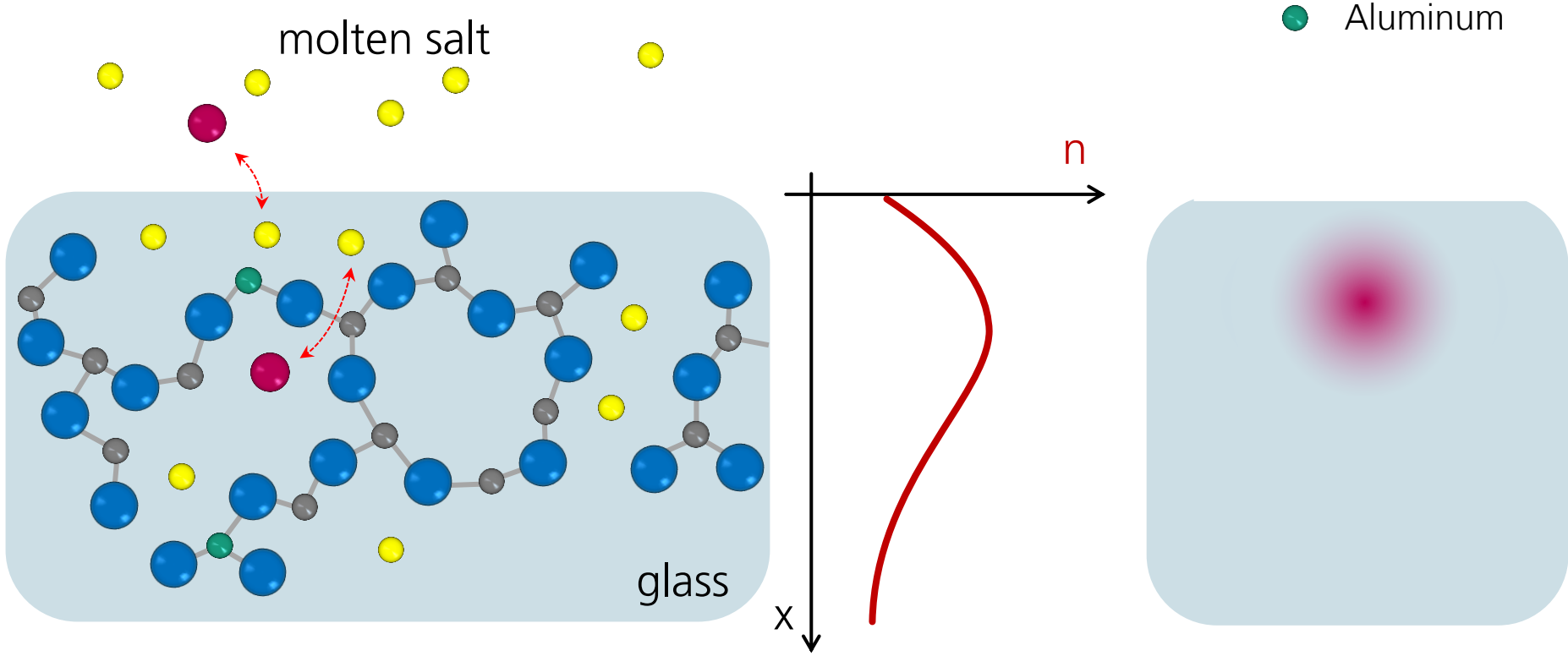
Optical Waveguides in Glass – Ion Exchange

Burying the waveguides can be achieved with a second ion exchange.

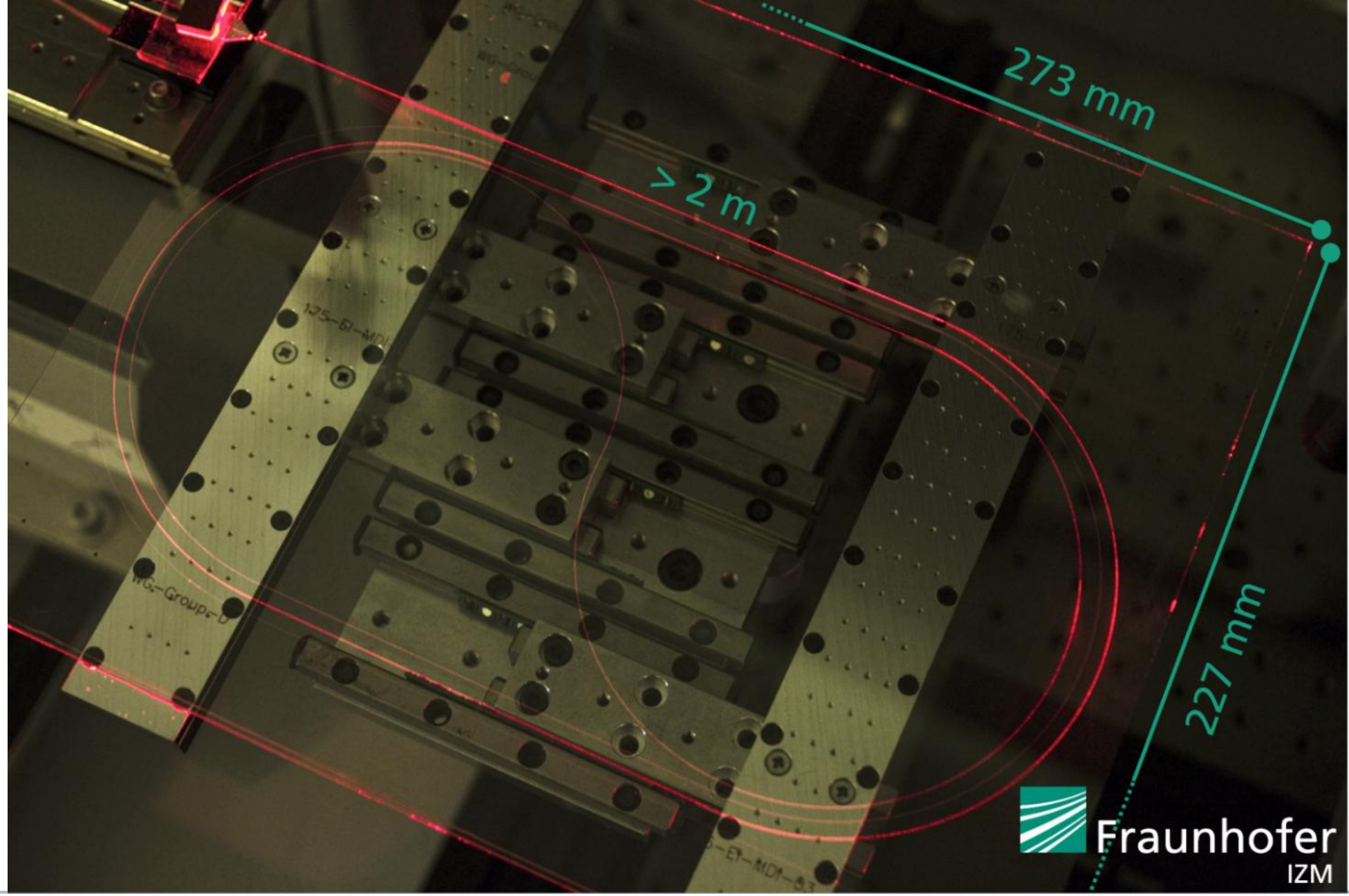
Sodium
Silver
Oxygen
Silicon
Aluminum

2) Reverse ion exchange to bury the waveguides



Waveguides
@ IZM

- $\alpha < 0.1$dB/cm @ 533 - 1550nm
- Single mode & multi mode
- Low coupling loss to fibers



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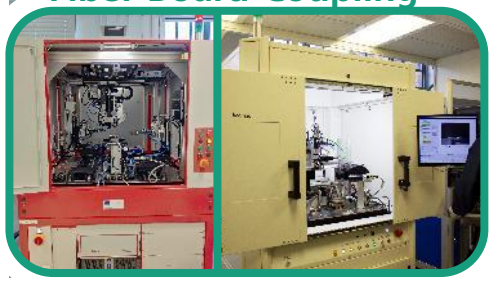
Fraunhofer IZM

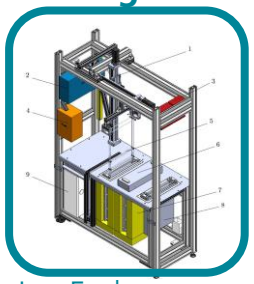
Optical waveguides in glass enable photonic GCS completely created at IZM

Fiber-Board-Coupling



Gluing, Welding

Waveguides



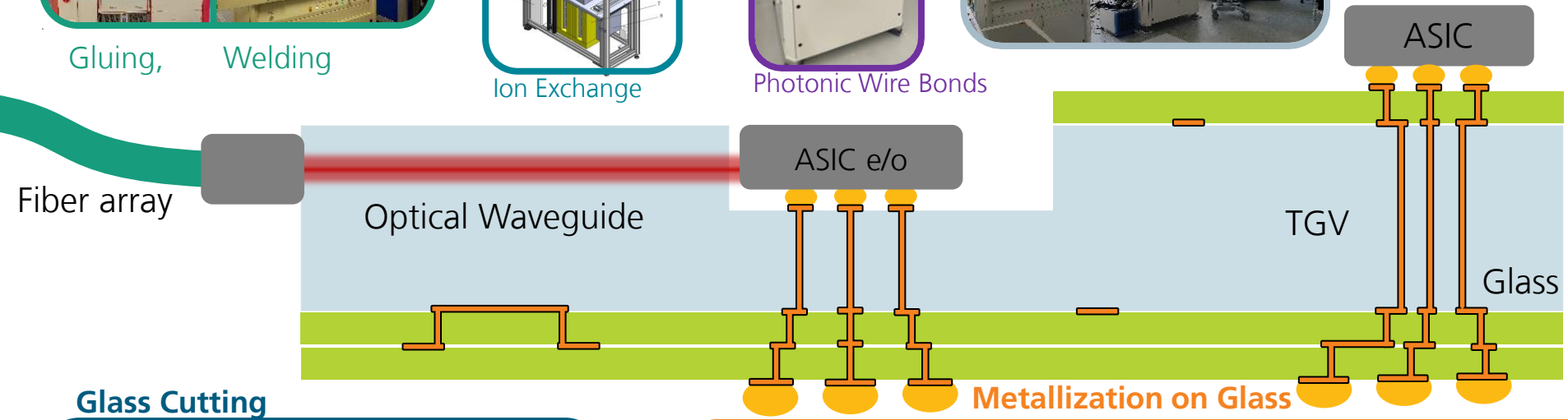
Ion Exchange

PWB

Photonic Wire Bonds

Chip Assembly

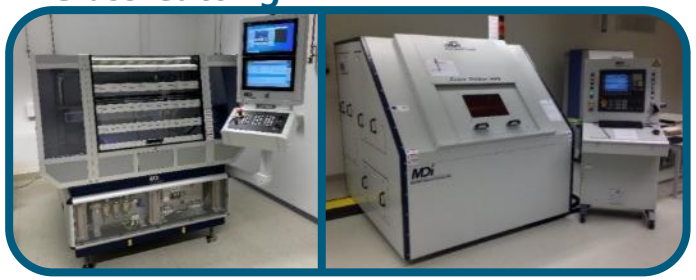
Glass Structuring



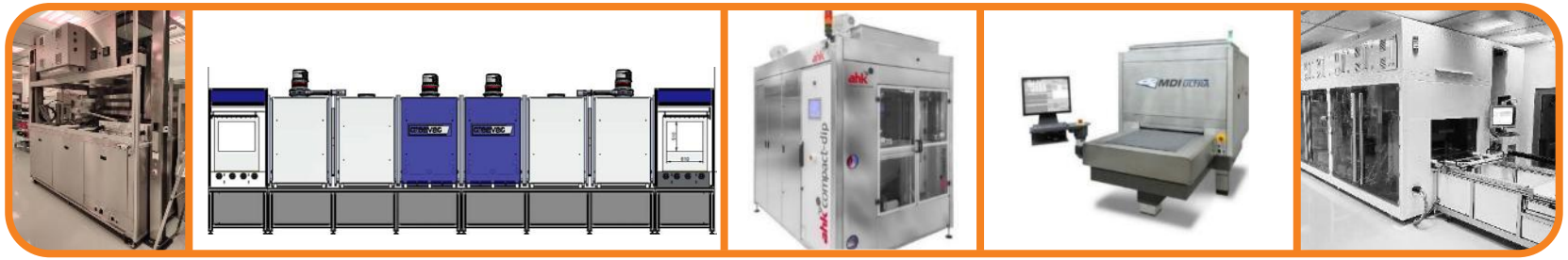
In addition:

- Testing: waveguides & electrical circuits, mechanics
- Inspection: AOI, REM, FIB, …
- Layer deposition: Lamination, PVD, CVD
- Etching: KOH, Plasma, molten salts, ….

Glass Cutting



Blade, Wheel, CO2-Laser



Cleaning, Sputtering, Coating, LDI, Plating & Etching

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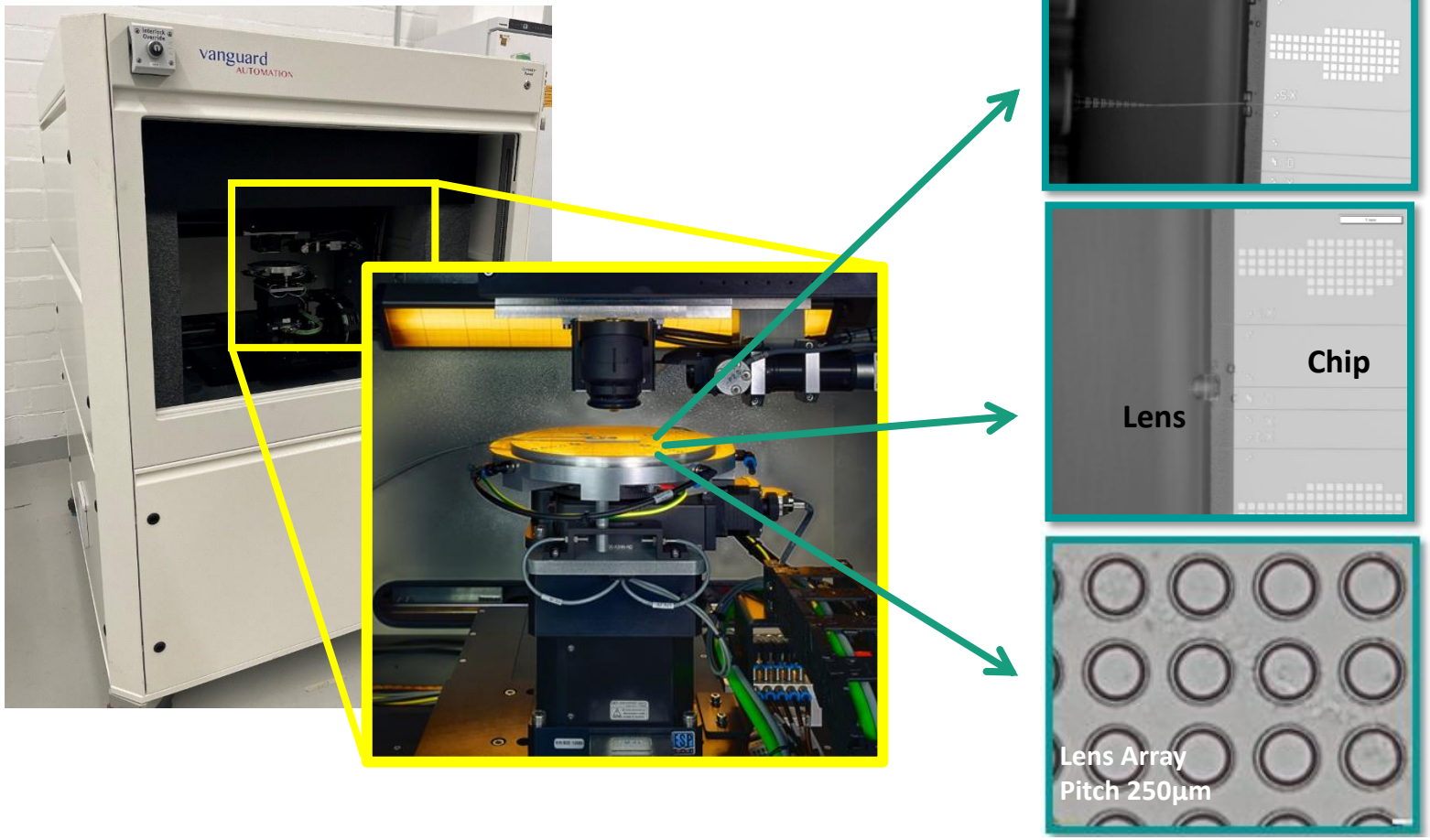
Printed 3D optical interconnections

Two-photon polymerization (2PP) printing

- Hybrid integration of different PICs
- Various 3D shapes to adjust the mode field diameter from 2 λ to 10 µm
- Sample positioning resolution of < 20 nm
- Positioning accuracy (laser structuring) of <= 50 nm
- Scalability and reproducibility Suitable for processing 10” wafers
- Writing field of 390 µm x 340 µm



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Fraunhofer IZM

Glass Panel Technology Group

Fraunhofer IZM is the coordinator

More members will join in the next weeks!

Please feel free to contact us, if you are interested in joining.

Contact

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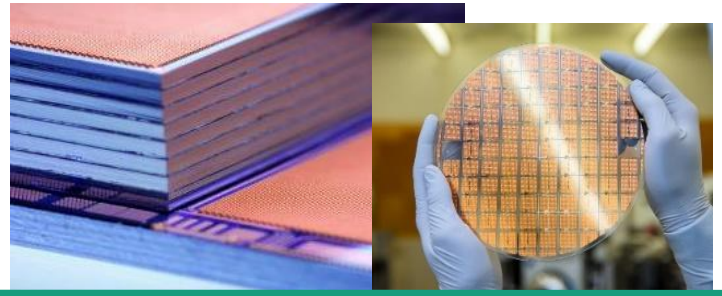
Photonics Systems for Massive Communications – CPO, Towards Photonics Chiplets

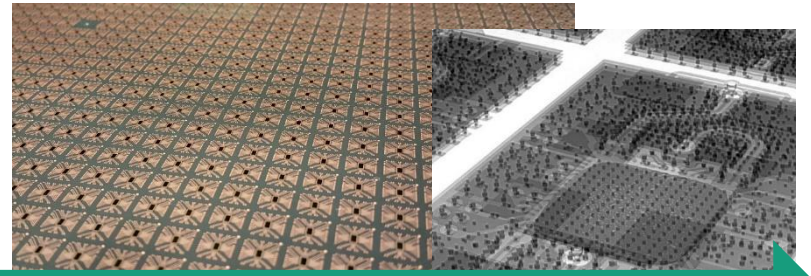
Bogdan Sirbu
Gr. Photonic & Plasmonic Systems
Dept. Wafer Level System Integration
Fraunhofer Institute for Reliability and Microintegration (IZM), Berlin

FMD visit to Nijmegen – Enschede

Wed.-Thur., 10-11 December 2025

Fraunhofer IZM – from Wafer- and Panel-Level System Integration





CMOS Feature Sizes 5 nm … >100 nm

WLP Feature Sizes 0.75 µm … >10 µm

PLP Feature Sizes < 5 µm … 100 µm

Wafer Level Packaging (WLP)		Panel Level Packaging (PLP)
Based on thin film materials & equipment	**Technology**	Based on PCB materials & equipment
100mm … up to 300 mm	**Format**	up to 610 x 456 mm²
CMOS – III / V - WBG wafers	**Input**	CMOS - III / V - WBG dies (w/ bumping)
2.5D / 3D integrated systems or system components	**Output**	Packaged / embedded modules

Fraunhofer IZM

Fraunhofer IZM – Department WLSI

Infrastructure & Process Capabilities

ISO 9001-certified process lines at two locations (Berlin & Dresden) for process development, material and equipment evaluation as well as R&D and industrial services on automated and semi-automated production equipment

Berlin: Vast variety of materials, processes and wafer materials / sizes suited for R&D prototyping and small volume manufacturing

Dresden: Industry-compatible process line for 200 / 300mm Si and glass wafers and prototyping for small to medium volume manufacturing

Berlin

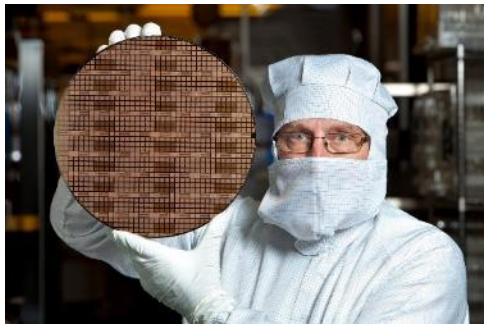
ISO 9001 2015 CERTIFIED

Dresden

Fraunhofer IZM (Berlin)

1000 m² clean room area (ISO 4-6)
Wafer sizes: 100, 150, 200 mm (partially 300 mm)

Fraunhofer IZM-ASSID (Dresden)



900 m² clean room area (ISO 4-6)
Wafer sizes: 200, 300 mm

Fraunhofer IZM

Heterogeneous Integration on Wafer Level

Research Focus @ WLSI Berlin

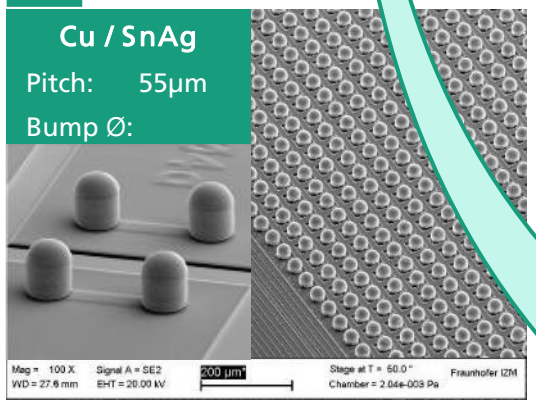
- **Advanced interconnect** solutions for optoelectronics, RF and MEMS packaging and power interconnects (Cu/Sn(Ag), Cu/Sn, Ni/Au, Au, AuSn, nano-porous Au (NPG), In, InSn)
- Temporary/Permanent **wafer bonding** (adhesive, solder, anodic, direct)
- High density **flip-chip assembly** (D2D, D2W)
- **2.5D / 3D integration** (WL SiP, CSP)
- **Silicon interposer** with high density, multi-layer RDL with application specific TSV integration (via middle, via last, back side TSV) and **Glass interposer** with with high density, multi-layer RDL and TGV
- **Fan-In and Fan-Out wafer level packaging** (RDL first/last, multi chip (Si, GaN, SiC, …)) with high density RDL first/last
- **Detector module** flip-chip interconnects and assembly
- Wafer level **MEMS packaging** and prototyping of MEMS sensors
- Development of **opto-electronic systems** (design, hybrid integration, characterization)

Pitch / Material Progression to Ultra-Fine Pitch

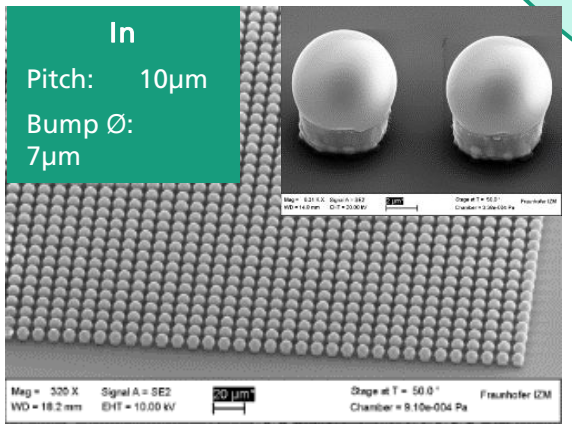
Bumping and Assembly Technology

Interface	Bonding Method / Interconnect	Material
Solder	Reflow Soldering, Self-Alignment	SAC, SnAg, AuSn
Solder	TC Bonding: Cu-Pillar/Sn, PAUF	Cu-Pillar/Sn
IMC	Transient Liquid Phase Bonding („SLID")	Cu/Sn, Au/Sn
IMC	Solder Diffusion Bonding (solid/solid)	Cu/Sn, Ni/In, Ag/In
Metal	Metal TC Bonding (solid/solid)	Cu-Cu, Au-Au, In-In
Metal	Nanoporous Gold (NPG)	NPG
Dielectric/Metal	Hybrid Bonding	Cu/SiO, NPG/Polymer
Bump Pitch, µm	1 3 5 7 10 20 30 50 70 100	

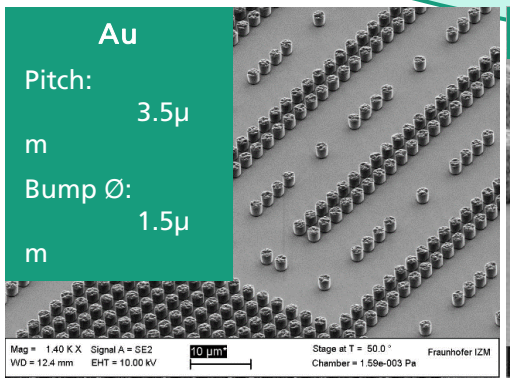
Cu / SnAg
Pitch: 55µm
Bump Ø:



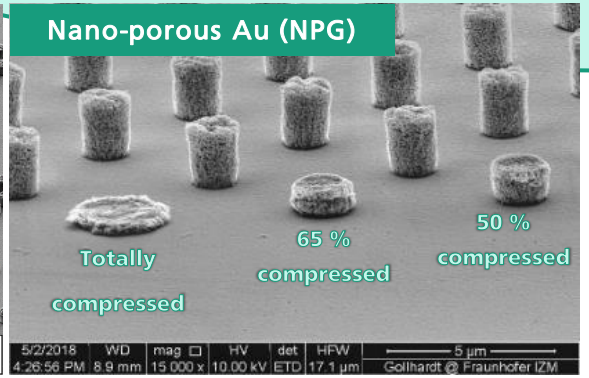
In
Pitch: 10µm
Bump Ø: 7µm

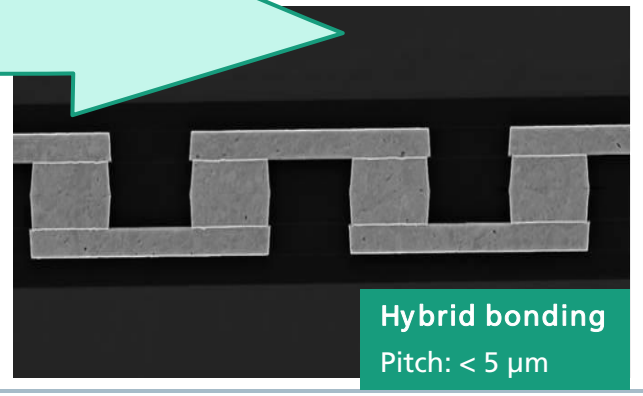


Au
Pitch: 3.5µm
Bump Ø: 1.5µm



Nano-porous Au (NPG)





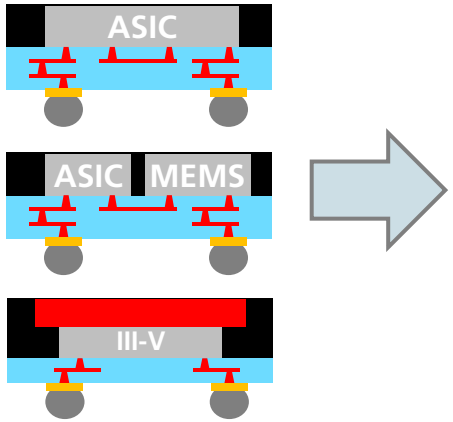
Hybrid bonding
Pitch: < 5 µm

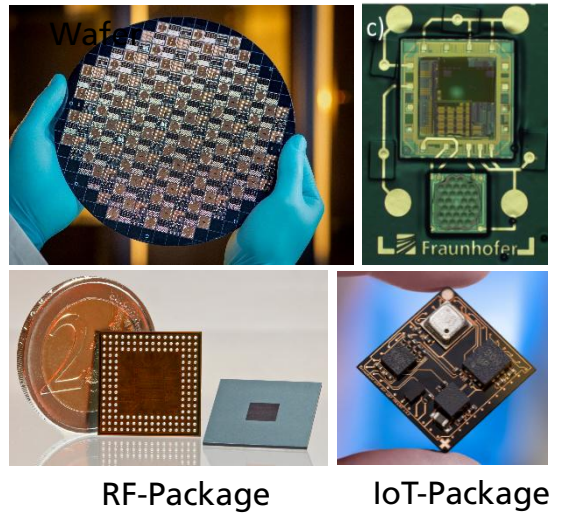
Interposer and Embedding Substrates

MATERIAL SELECTION

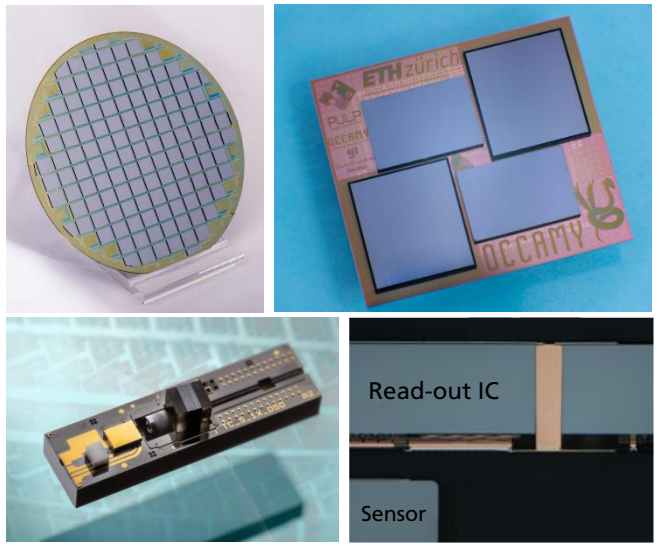
- Process ecosystem: via generation (etching, laser), passivation (CVD, polymer), electro-plating, temporary carrier bonding, wafer thinning, wafer bonding
- Applied material compliments / enables functionality or robustness for specific applications (co-design)

Epoxy Molding Compound

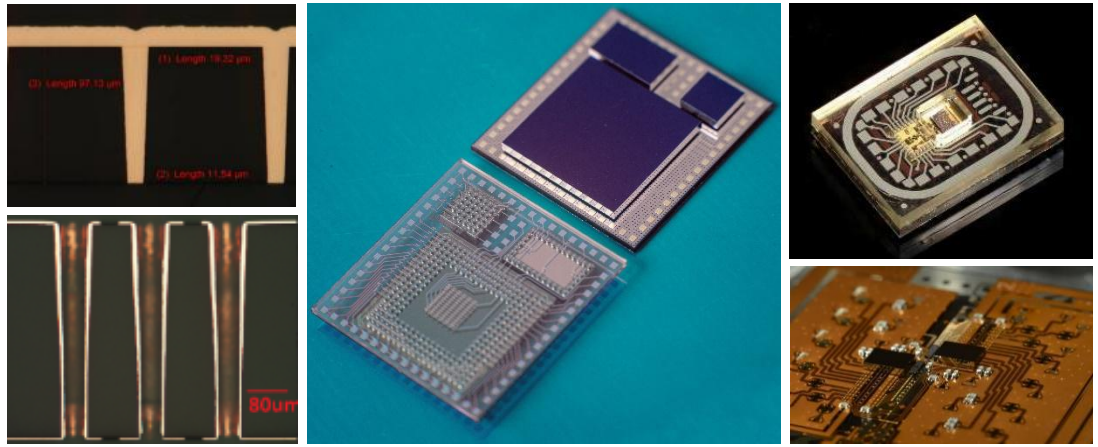




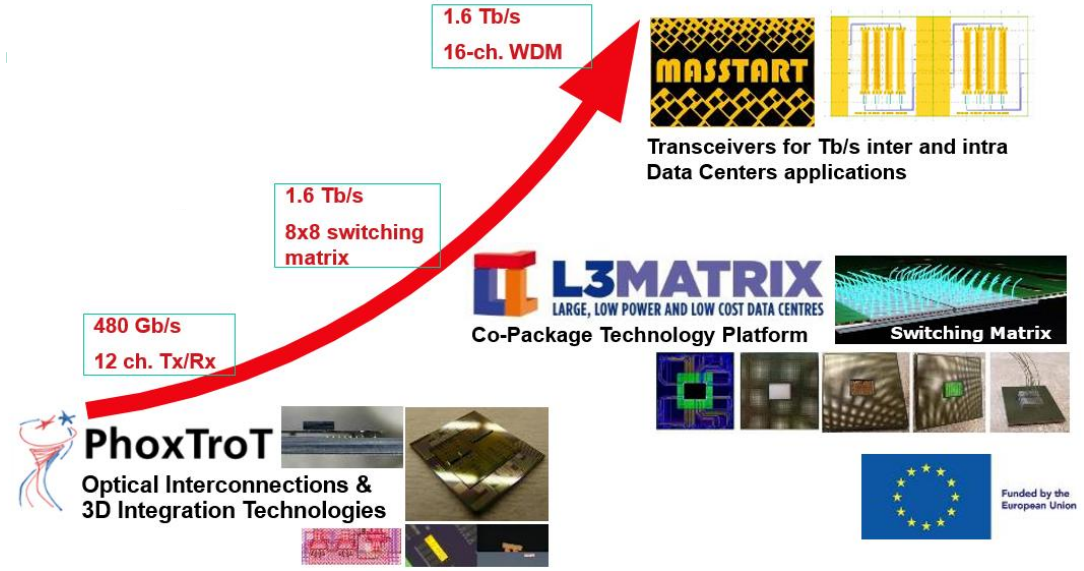
Silicon

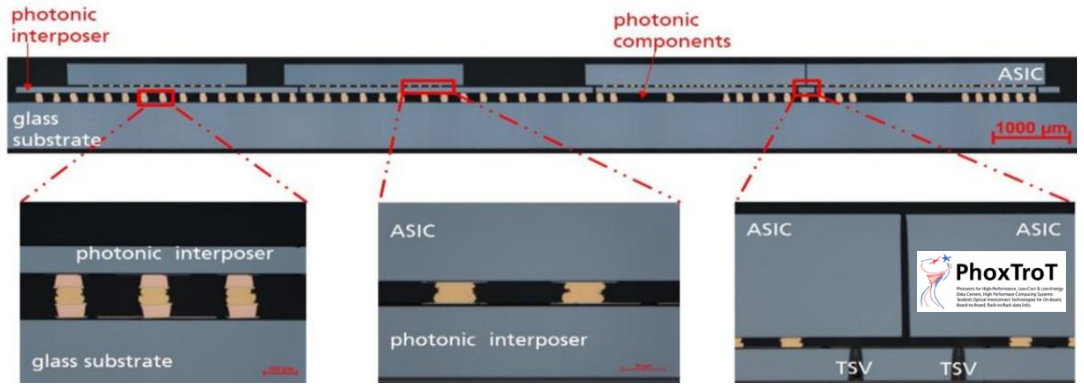


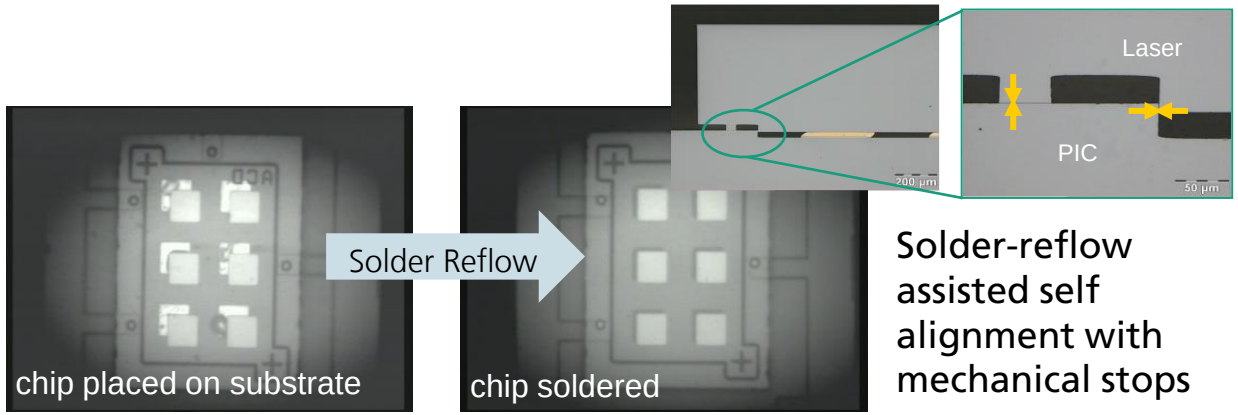
Glass



Photonics System Integration





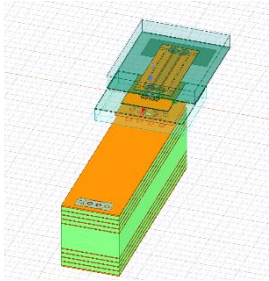


Solder-reflow assisted self alignment with mechanical stops

- Photonic Interconnects for Data Centers
  - High data rate communication using Photonic IC (PIC)
  - Drivers in Industry: next generation computing - cloud, edge, node HPC
  - Electrical and optical integration on silicon photonic interposer and PIC
  - Optical off-chip interconnection for chip-to-chip communication: low-latency, high-bandwidth, high density, low power
  - Massive switching beyond 400 Gb/s with new developed serializer/deserializer (SerDes) circuits and optical links

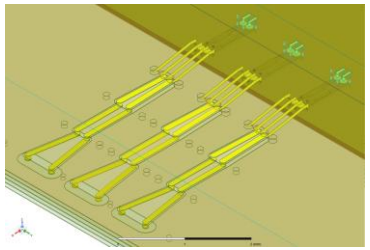
Photonics Value Chain addressed at Photonic and Plasmonics System (PPS)

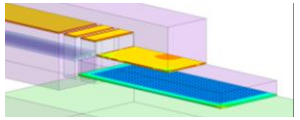
HF simulations

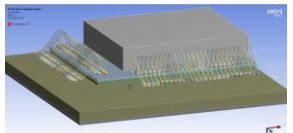


Routing

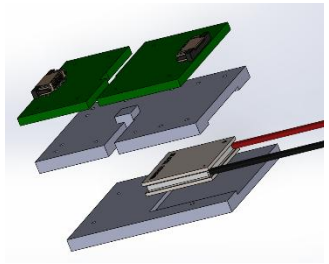
System Integrity



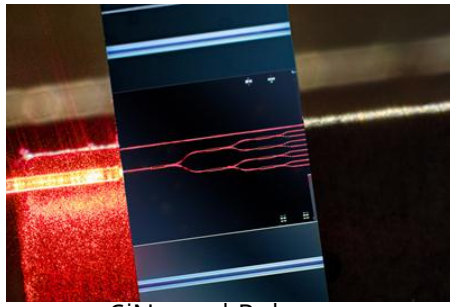




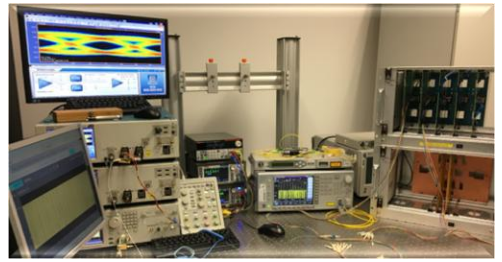
Thermo-mechanical simulations

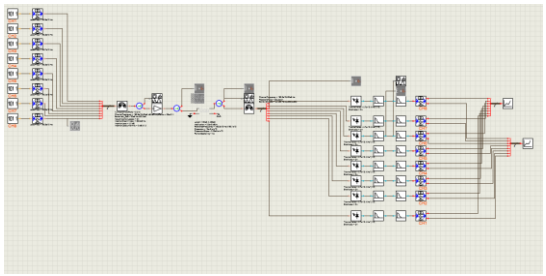


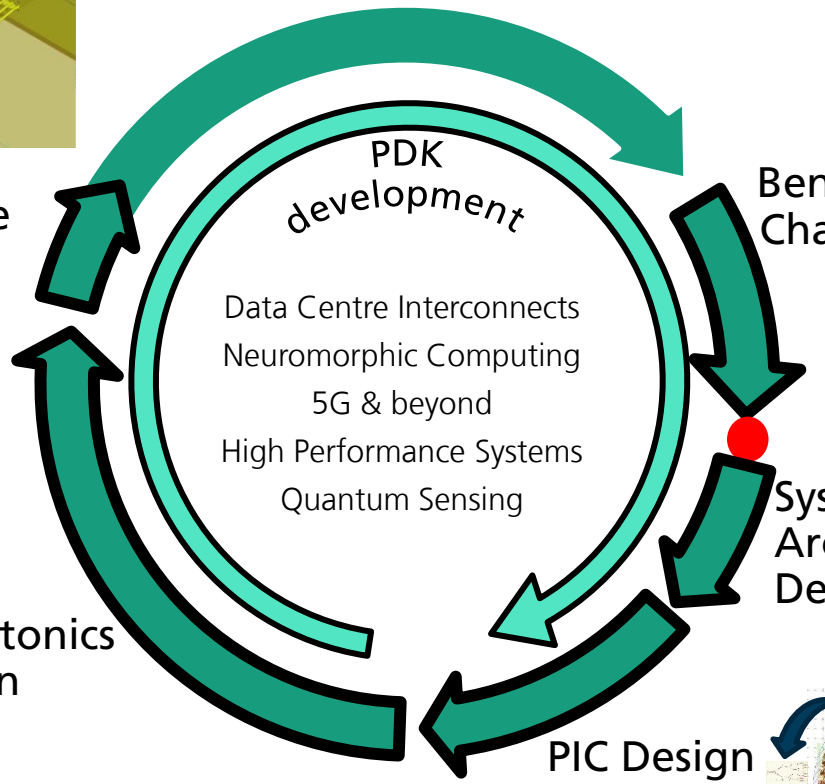
Thermal management



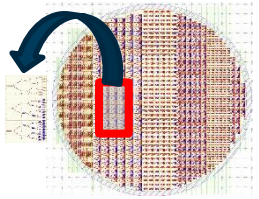
SiNx and Polymer waveguide fabrication



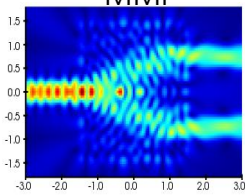




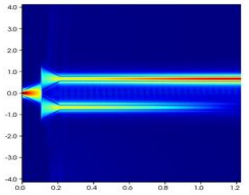
LIDAR



Inverse design MMI



MO dielectric switch / isolator

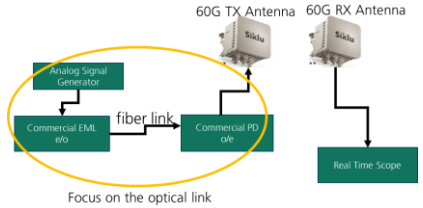


From Waveguides to PIC-Architectures

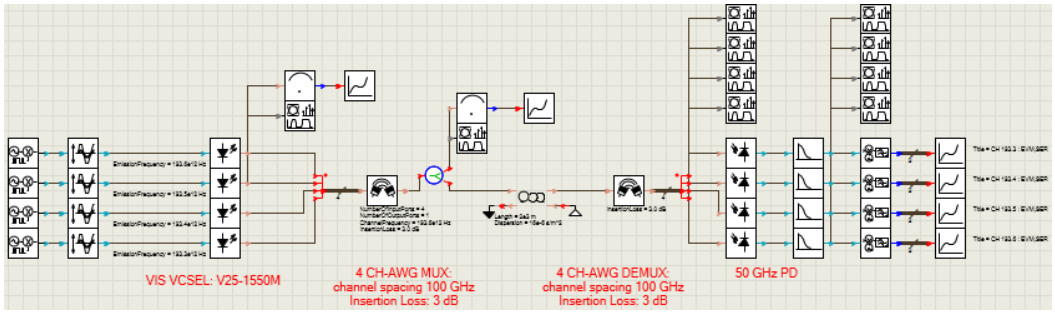
Fraunhofer IZM Design and Characterization expertise 1/2

System Level / Architecture Design

- Use case centric
- Application feasibility
- Overall system key performance indicators evaluation (power budget, latency, BERT, SNR, SFDR…)

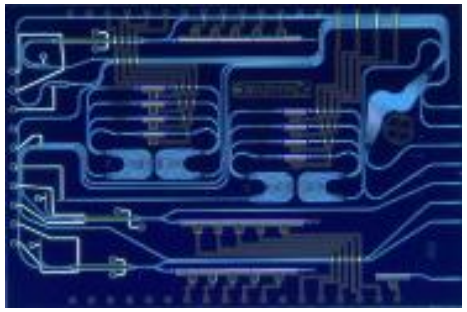


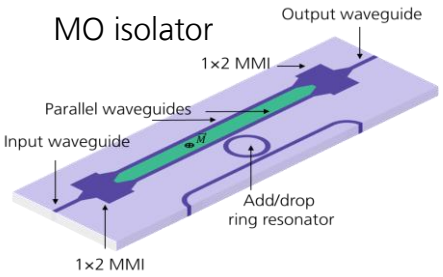
4 ch DWDM OFDM Analog Radio over Fiber system



PIC Design

- Technology agnostic (Si Ph, SiNx, InP, SiC, polymer, glass, free-space)
- Multi platform integrated layout generation
- Building block optimization
- Customization of optical specs to meet performance criteria
- Optimization of source to chip and interlayer coupling schemes
- Simulation and design of optical-wireless communication links





From Waveguides to PIC-Architectures

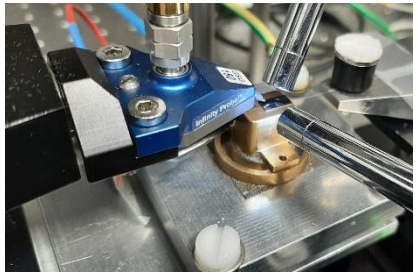
Fraunhofer IZM Design and Characterization expertise 2/2

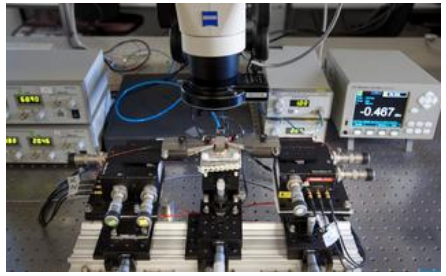
Package Design

- Assembly process flow definition
- Thermo-mechanical constrains evaluation
- Thermal management implementation on the package
- Signal integrity analysis, crosstalk evaluation between channels
- Power integrity of the package
- HF transmission line design and optimisation
- Routing
- Interfaces design (optical, RF, electrical, interconnects)
- Cost analysis, feasibility study

Benchmarking & Characterization

- Photonic integrated circuit performance evaluation (loss, power consumption, bandwidth, jitter, static, dynamic, …)
- Benchmarking of Data Centre Interconnects
- System performance evaluation (power budget, latency, BERT, SNR, SFDR…)
- High frequency characterisation of materials, components, and subsystems (up to 300GHz)
- Microwave photonics testbed



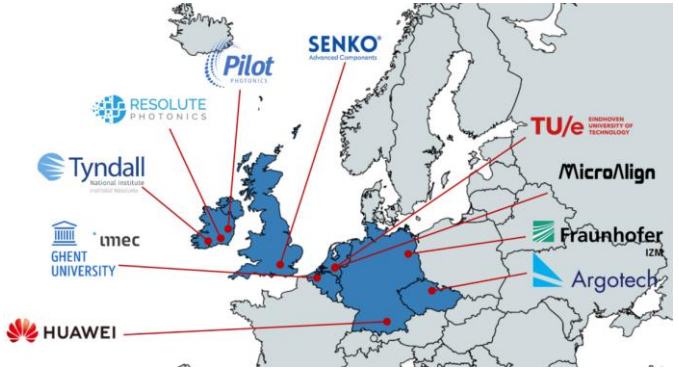


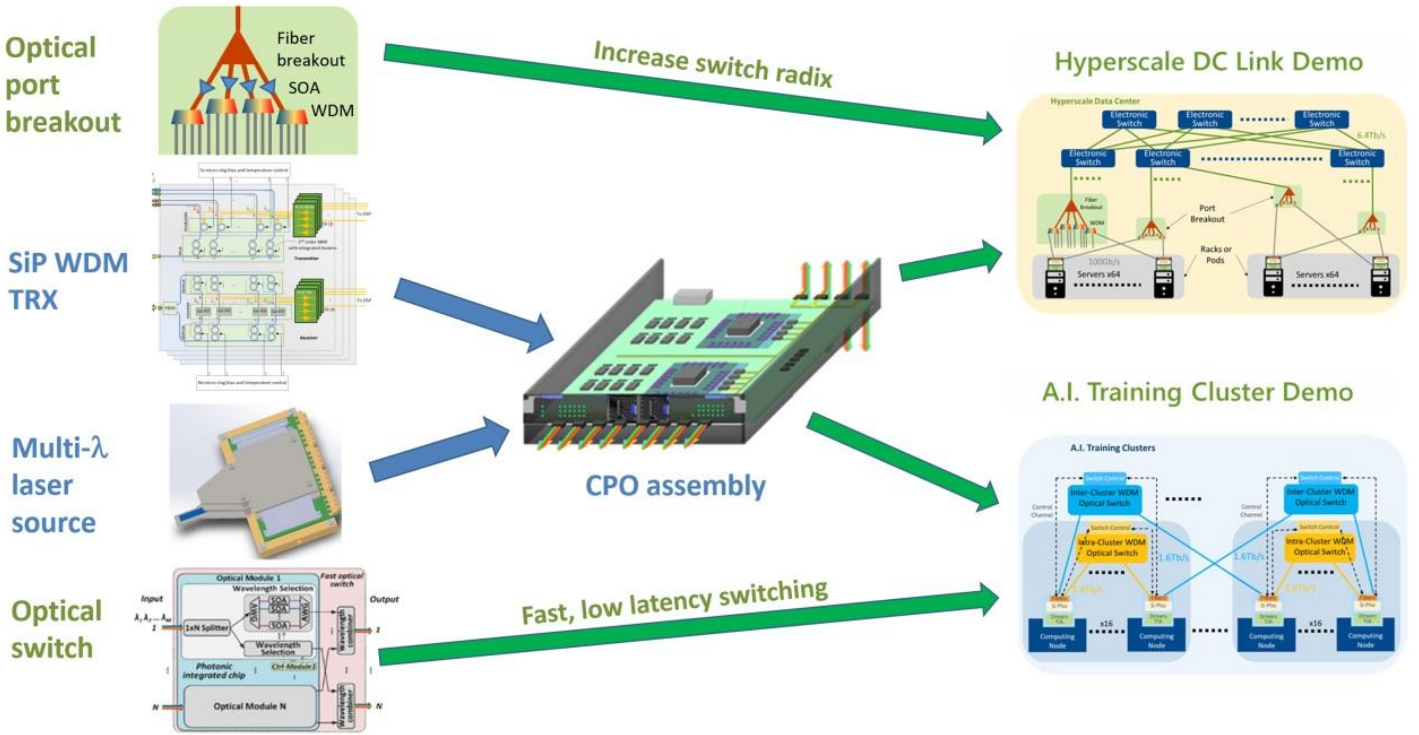
Fraunhofer IZM

ADOPTION

Project Ambition

- Create a European ecosystem/value chain around CPO from chip fabrication, to advanced assembly, system integration and the deployment by cloud computing operators.
- Low power (3pJ/bit), low cost (<0.5€/Gbps) switching solutions for intra-data centre networks targeting beyond 204.8Tb/s switches and an increased switch radix.
- Advanced packaging and high-efficiency fiber coupling
- All-optical circuit switches with ns-switching time
- Contribute results to standardization – training – synergies with other EU consortia



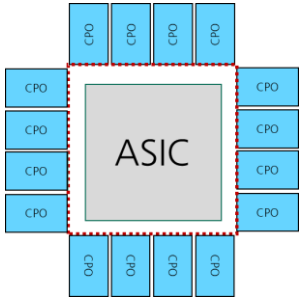


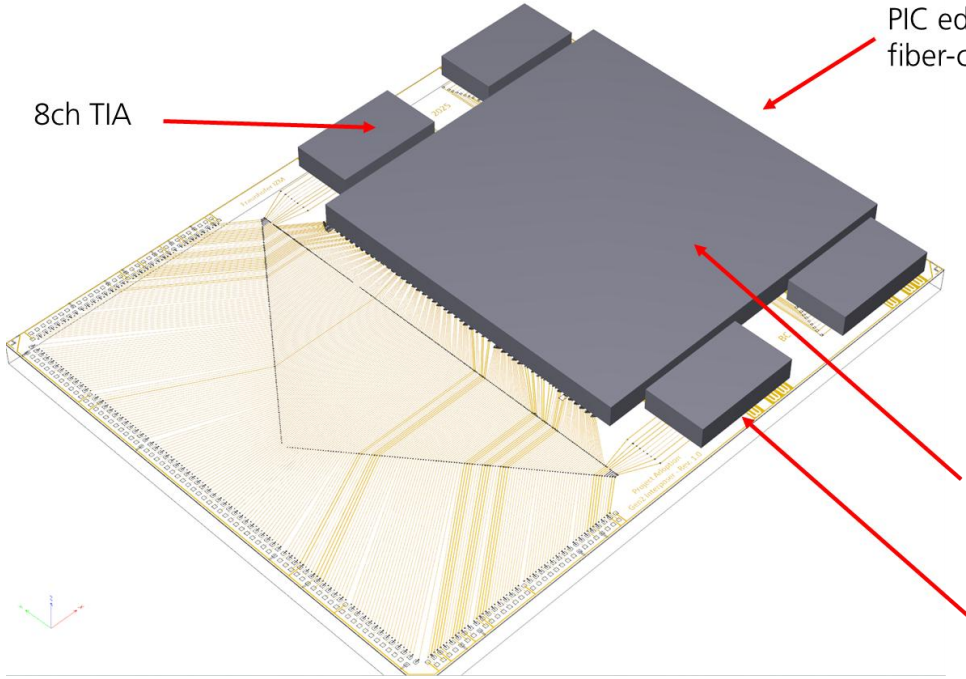
ADOPTION

Next Generation: 204.8Tb/s switches for AI data center

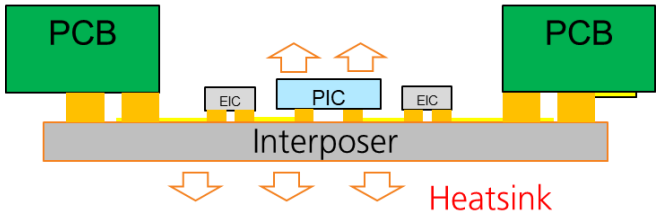
2023-2026

- Silicon interposer 32ch PIC 112Gb/s/ch
- Create a European **ecosystem**/value chain around **CPO** from chip fabrication, to advanced assembly, **system integration** and the deployment by cloud computing operators.
- Low power (**3pJ/bit**), low cost (**<0.5€/Gb/s**) switching solutions for intra-data center networks targeting beyond **204.8Tb/s** switches and an increased switch radix.





x4



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Fraunhofer IZM

Photonic & Plasmonic Systems

ENGINEERING PHOTONIC SOLUTIONS

THROUGH CUTTING EDGE RESEARCH

INNOVATING TOMORROW'S PRODUCTS

Contact

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Leibniz Institute
for high
performance
microelectronics

SiGe Photonics
IHP opto-electronic RF technologies

Lars Zimmermann

APECS/FMD Workshop

Nijmegen | December 10, 2025

Intro / background

innovations
for high
performance
microelectronics

Fak. IV, FG Silizium-Photonik, TU Berlin

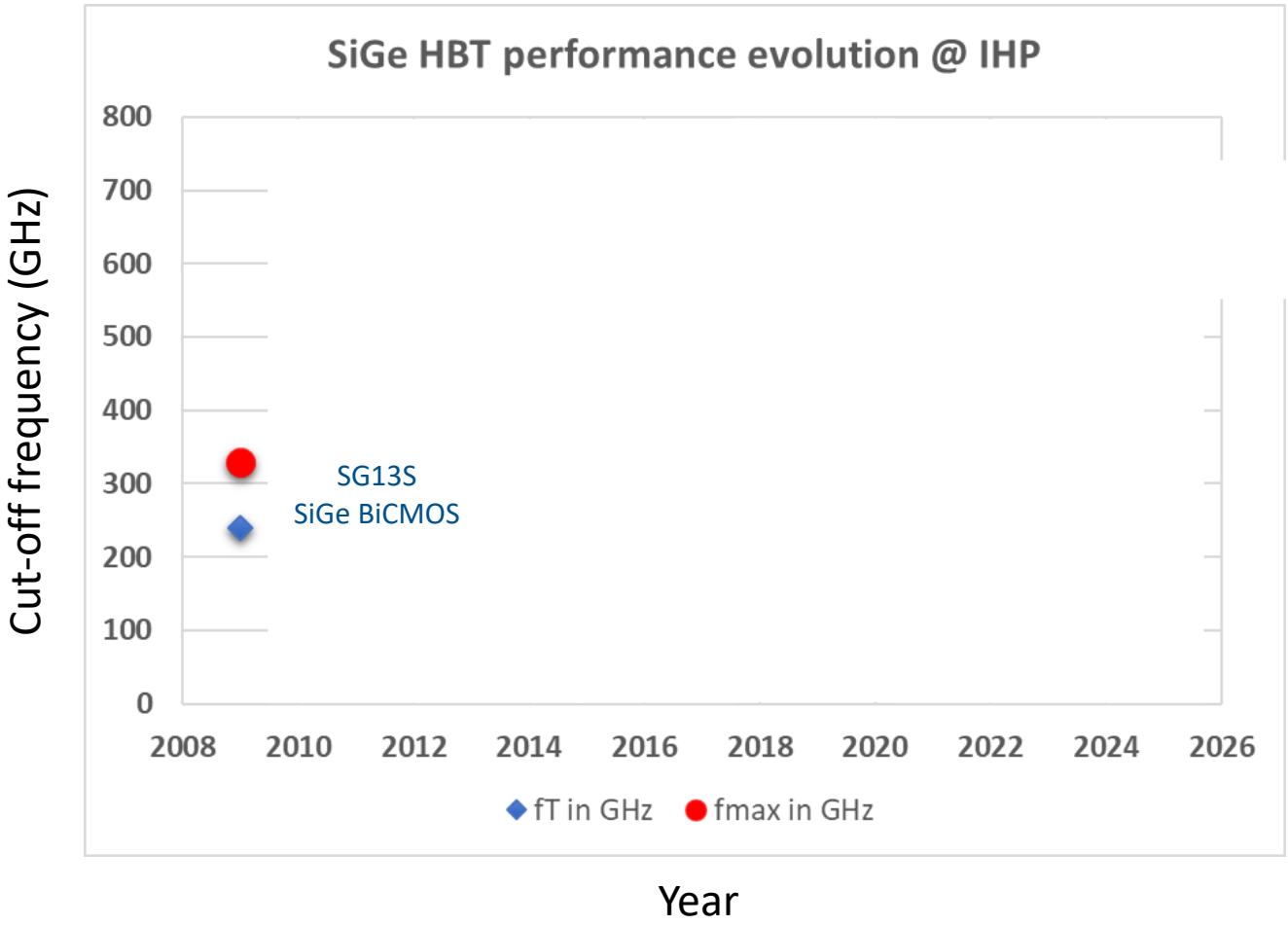
Group: Si Photonics, IHP, Technology Department

IHP is a research foundry

- Cleanroom area
  - 1500m² class 1 for 100wspw
- Technology & operation
  - RF SiGe BiCMOS @ 24/7 mode
- Technology level
  - 200mm @ 0.25µm & 0.13µm

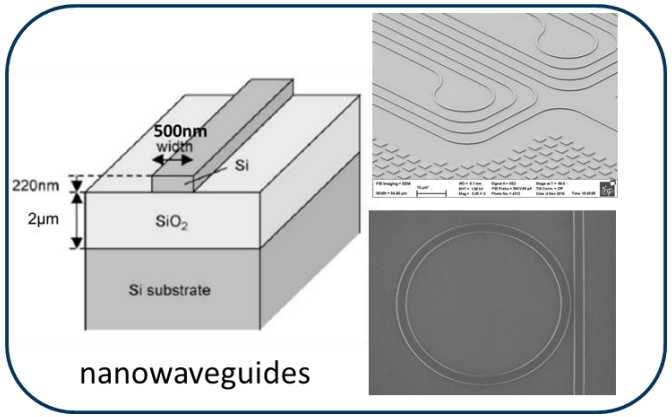
Silicon photonic + electronic technologies in MPW + low volume

SiGe HBT and BiCMOS | Evolution at IHP

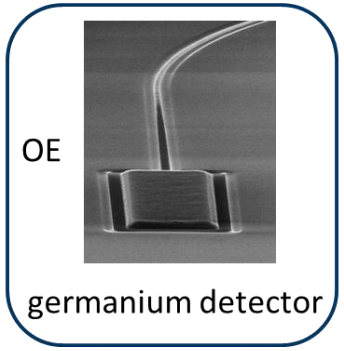


Monolithic – SG25H5EPIC – EPIC

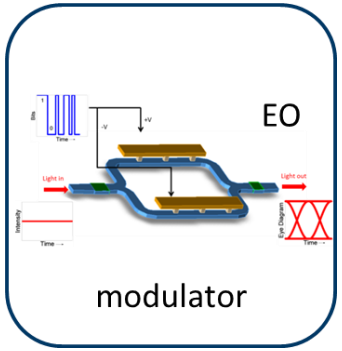
Integrated optics



Reception

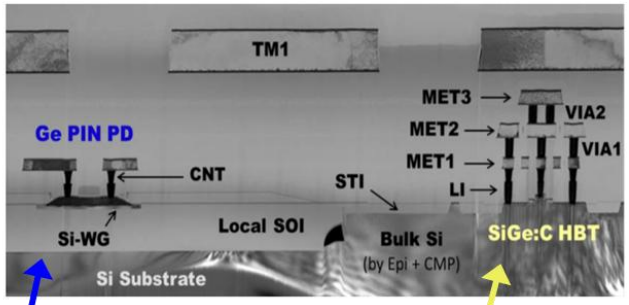


Modulation



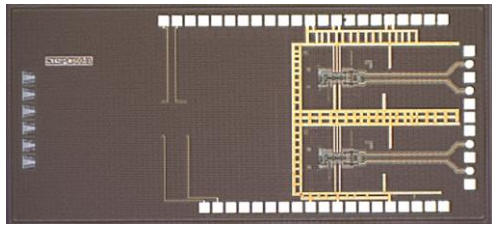
High-speed analog

- planar technology
- enabeling **ePIC**s = electronic photonic integrated circuits
- λ = 1200 – 1600nm



60 GHz Bandwidth Germanium Photo Diode

220 GHz f_T SiGe NPN
290 GHz f_{max}

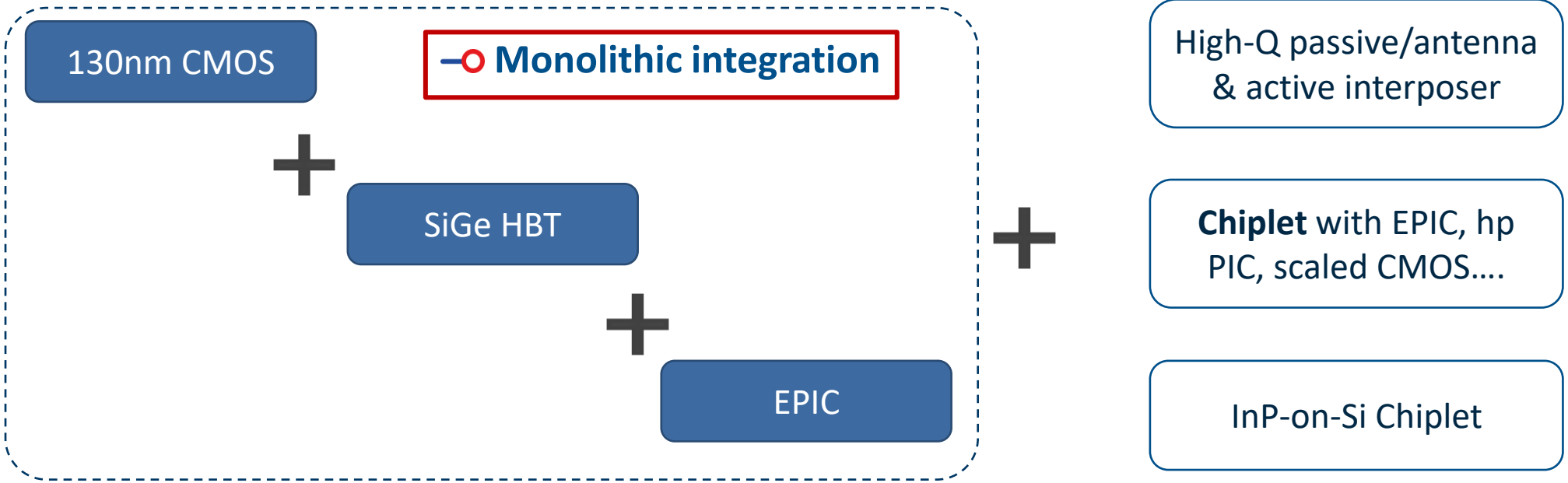


64 Gbaud coherent receiver EPIC

64 up to ~ 80Gbaud

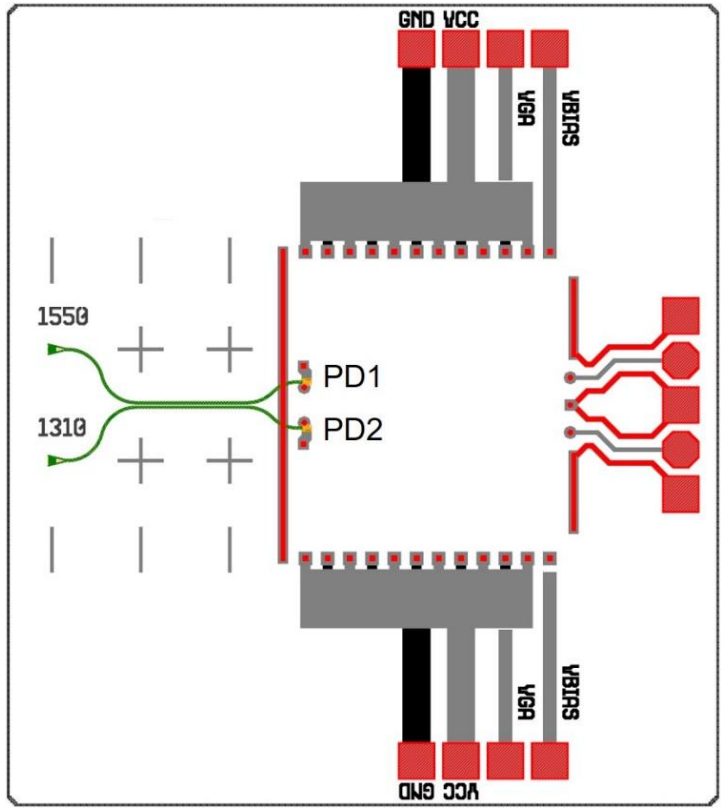
CMOS + X @ IHP

*Chip-to-wafer & W2W integration towards **Quasi-Monolithic-Integration***

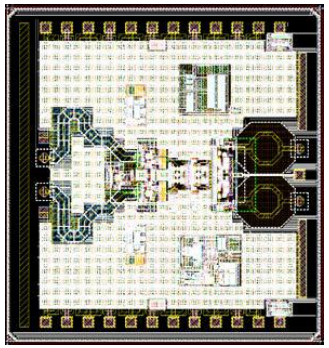


Aluminum-aluminum stacked receiver

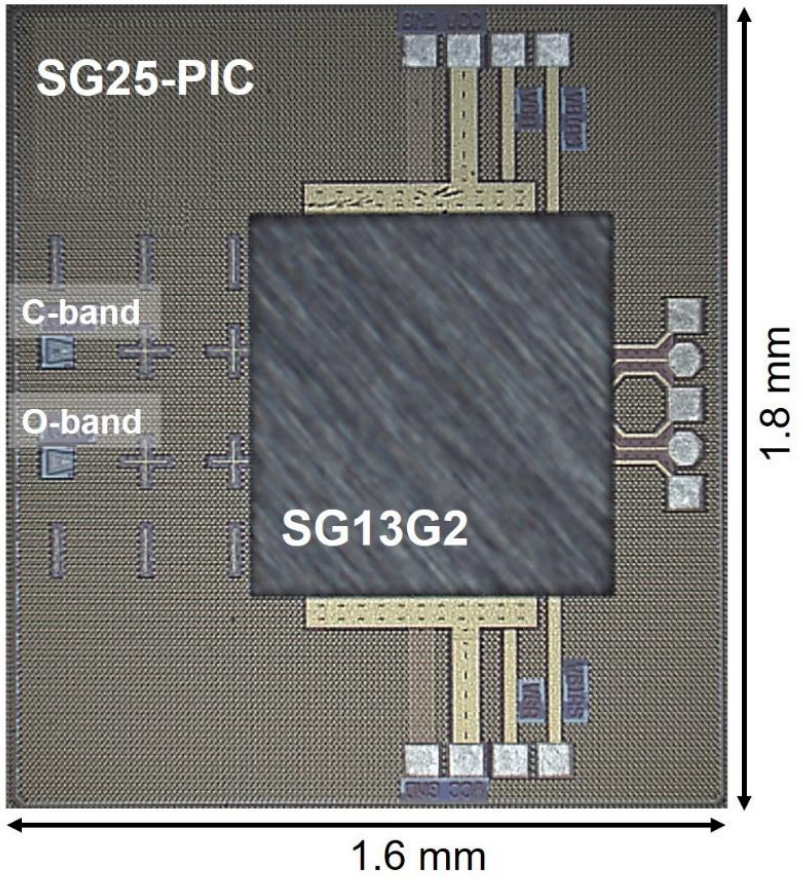
PIC - design



EIC - design



after bonding ….

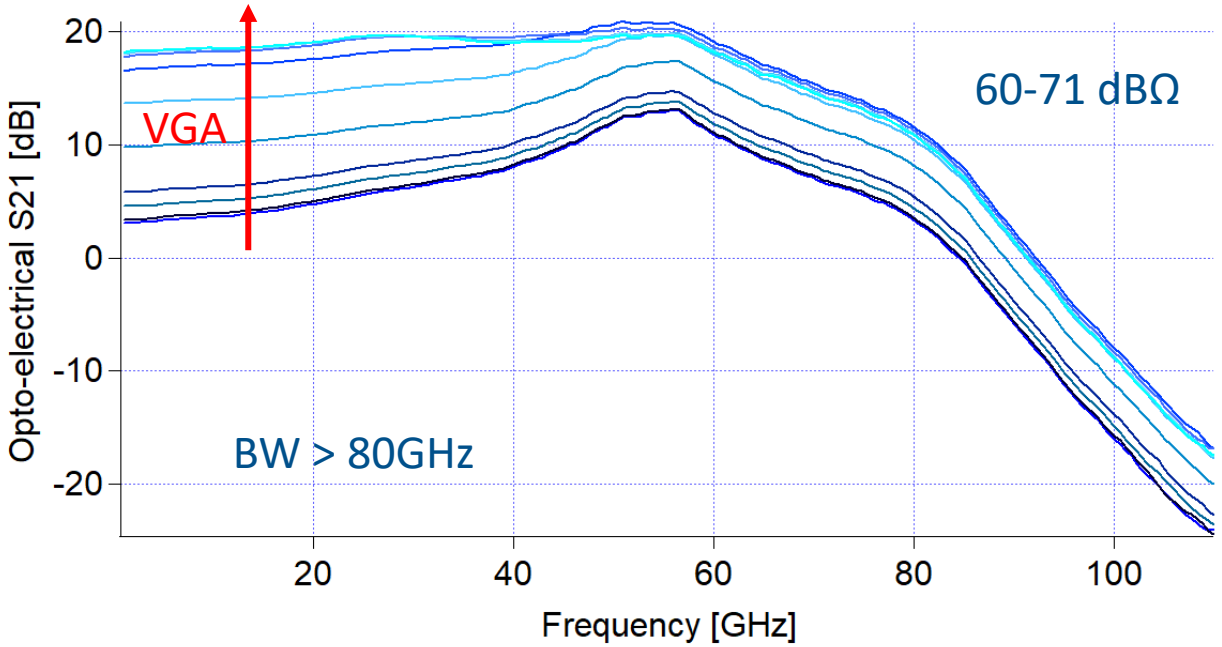


Bonding pad size: 20 µm

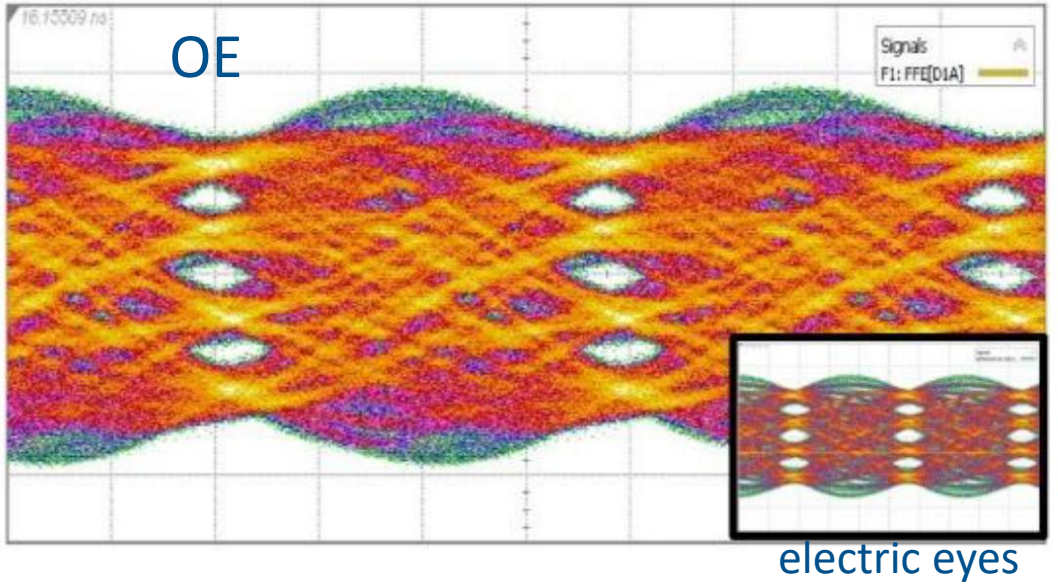
Anna Peczek et al., 132 GBaud PAM4 IM/DD Silicon Receiver Subassembly Realized by Stacking Technology, IEEE JLT,2025

Stacked assembly characterisation

- OE reponse measured for different gain at 1310 nm



132 Gbaud



electric eyes

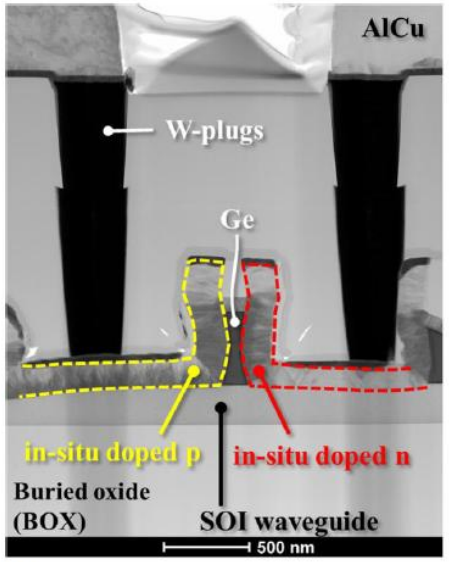
Anna Peczek et al., 132 GBaud PAM4 IM/DD Silicon Receiver Subassembly Realized by Stacking Technology, IEEE JLT, 2025

Power consumption: 385 mW

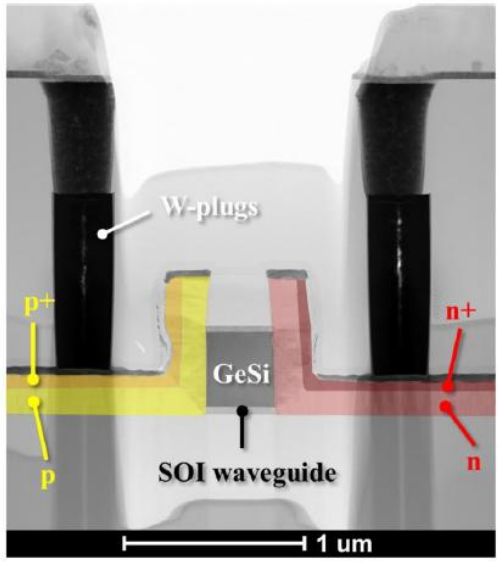
SiGe fin platform

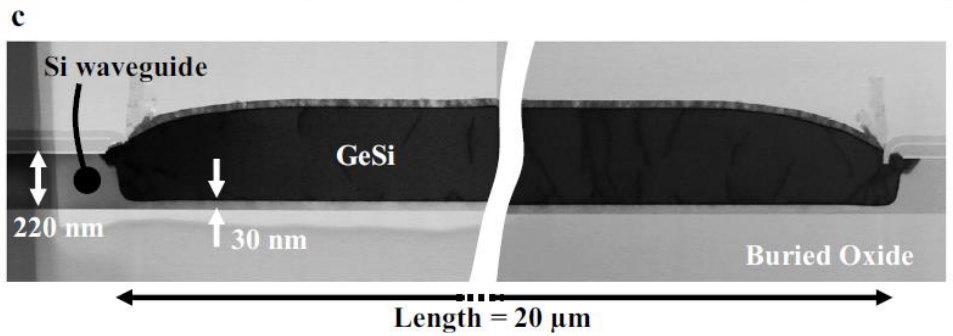
D.Steckler et al., Monolithic electro-optic platform on silicon with bandwidth of 100 GHz and beyond, Nat Commun 16, 10789 (2025) https://doi.org/10.1038/s41467-025-66566-2

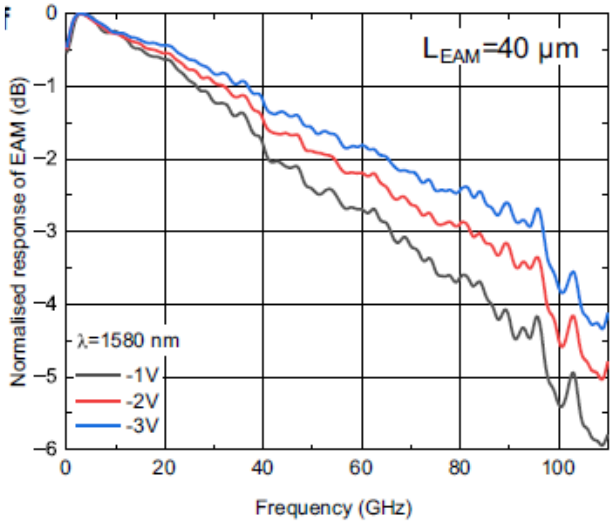
PD



EAM

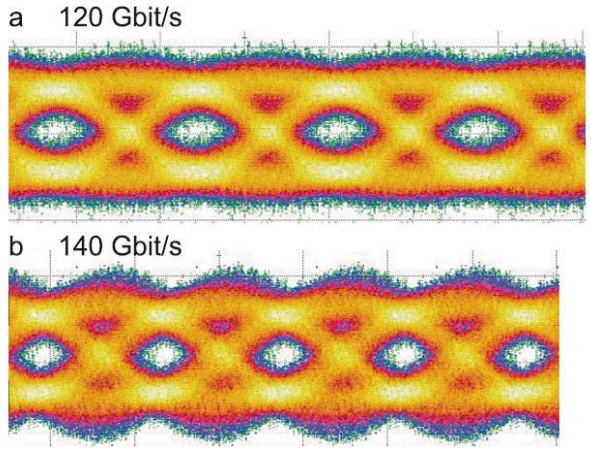






Vpp=2.4V

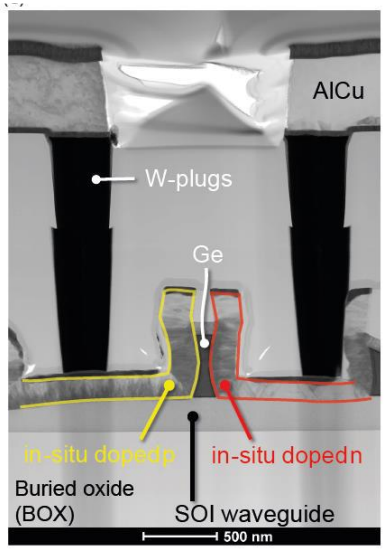
SiGe only measurement



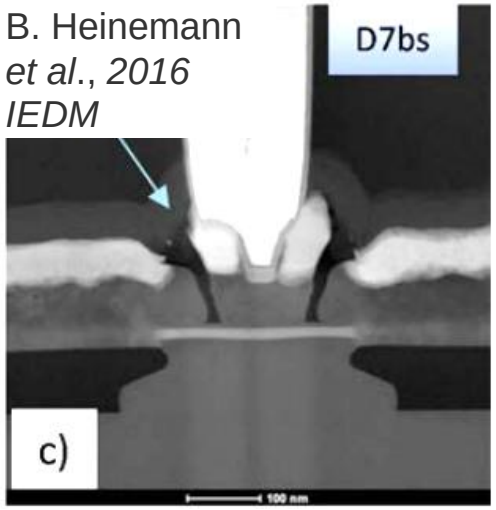
Next Generation of SiGe-Photonics at IHP

- Adaptation of SG13G3 SiGe HBT module into advanced ePIC technology

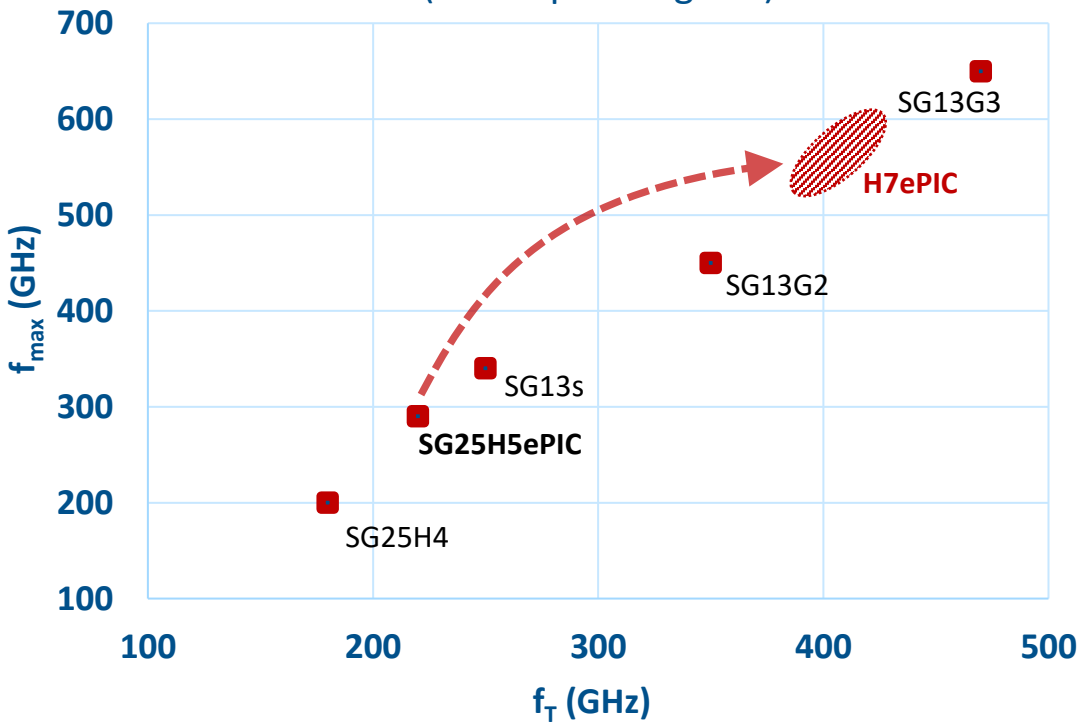
Ge-Fin photodiode



SG13G3 SiGe HBT



SiGe HBT performance
(development goals)



- **H7*e*PIC** and **H7PIC** with double Ge PD bandwidth > 100 GHz
- H7ePIC with double f_T
- First MPW in Nov 2025

Thank you for your attention!

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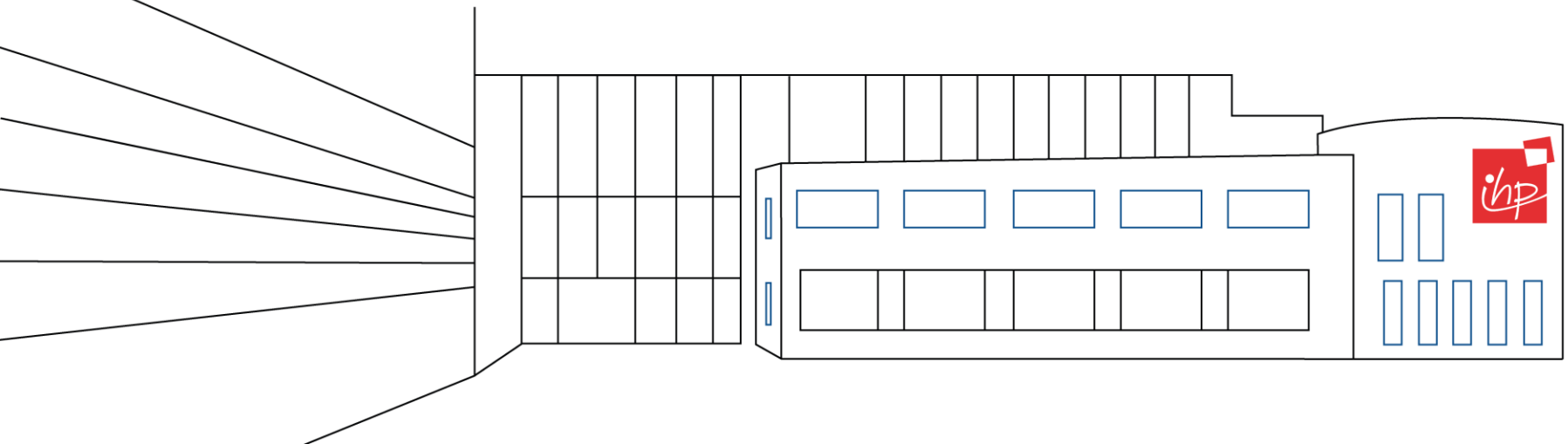
Im Technologiepark 25
15236 Frankfurt (Oder)
Tel.: +49 (0) 335 5625 407
E-Mail: lzimmermann@ihp-microelectronics.com



APECS

Forschungsfabrik Mikroelektronik Deutschland

Leibniz Association

Customizable 200 mm Wafer-Scale Post-CMOS Photonics Platform

Aleksandar Nesic

Fraunhofer IMS, Duisburg

Fraunhofer IMS

Fraunhofer Institute for Microelectronic Circuits and Systems IMS

UNIVERSITÄT DUISBURG ESSEN

Offen im Denken

Fraunhofer IMS, Duisburg

At a glance

Forschungsfabrik Mikroelektronik Deutschland

Fraunhofer Institute for Microelectronic Circuits and Systems (IMS)

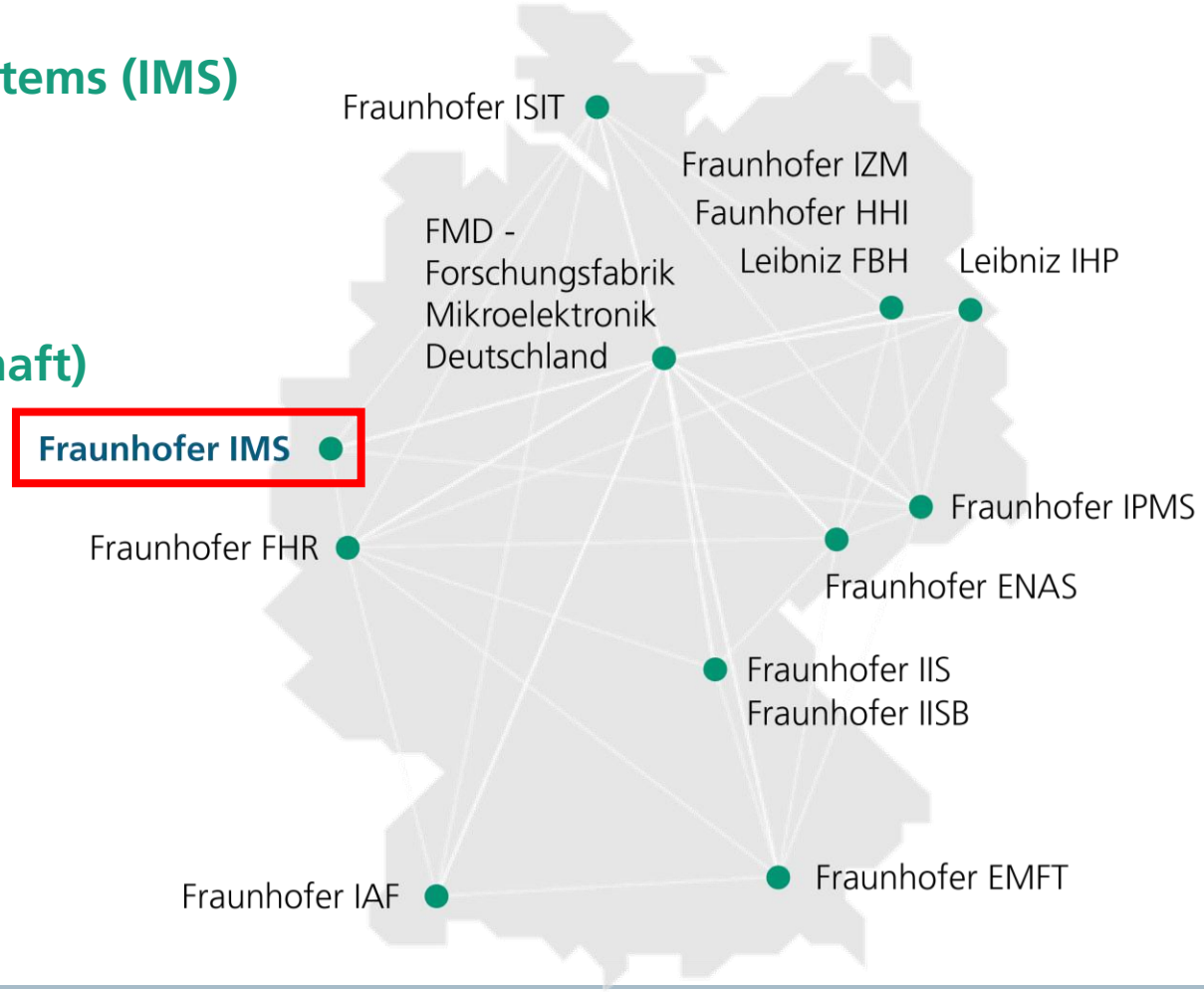
Duisburg, North Rhine-Westphalia
175+ employees, 30 M€ budget, founded 1984/85,
Director: Prof. Dr. rer. nat. Anton Grabmaier

Part of the Fraunhofer Society (die Fraunhofer-Gesellschaft)

Non-profit organization
76 institutes, 30.000+ employees, 2.9 B€ budget

Part of Fraunhofer Group for Microelectronics

11 institutes + 2 Leibniz institutes
coordinated from Berlin



Fraunhofer IMS

Fraunhofer IMS Technology Department

Research areas and groups

Semiconductor Integration Technology (SIT)

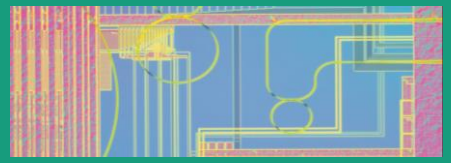
Detector Technologies

- CCD
- Single Photon Avalanche Diodes
- Bolometer / IR detectors

Pressure sensors

Post-CMOS wafer scale integration technologies

Photonic Integrated Circuits (PIC)



Waveguides

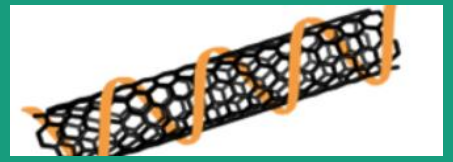
- Silicon nitride
- Aluminium nitride

Modulators

Nonlinear Devices

- Quantum photonics

Biomedical Nanosensors (BMS)



Carbon Nanotubes Biosensors

Biosensing for medical and environment diagnostics

Nanostructured Sensor Materials (NSM)

Material development for optical sensors and photonic devices

Functional materials for optoelectronics, novel compute

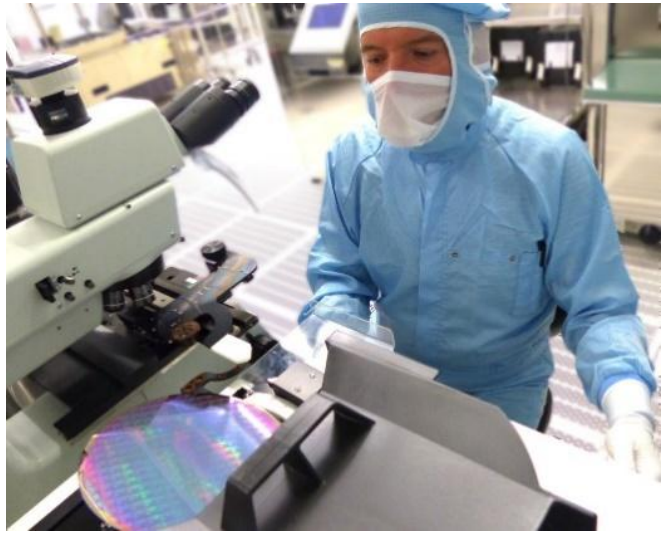
200 mm post-CMOS Photonic Platform

Our experience and infrastructure

1,900 m² ISO 4 and 400 m² ISO 6 cleanroom

ISO 9001 certified fabrication

Prototyping **from low-volume R&D** (<25 wafers) **to pre-series manufacturing** (~1000 wafers/year)



Open interfaces for integration

- Novel materials (2D, electro-optics, bio, …)
- Application specific components (microoptics, microfluidics, …)
- Chiplet and heterogeneous integration

In-house experience on **microelectronics + MEMS + PIC**

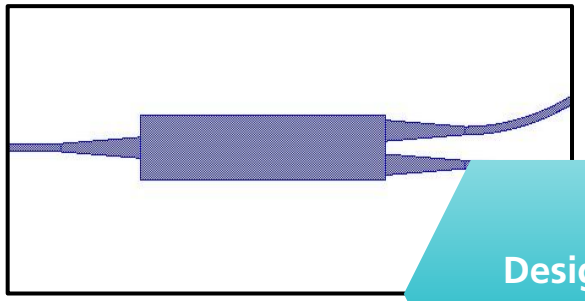
Long-standing experience in **post-CMOS integration**

Flexible design rules for application specific solutions

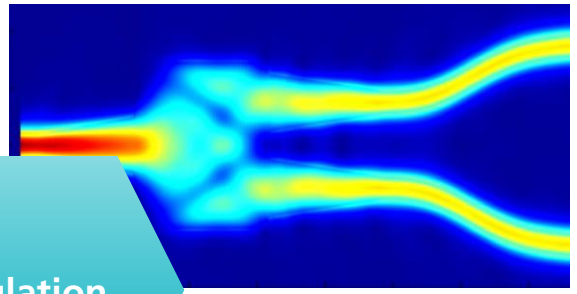
200 mm post-CMOS Photonic Platform

Supporting you from idea to pilot fabrication

We are an experienced upscaling partner for start-ups!

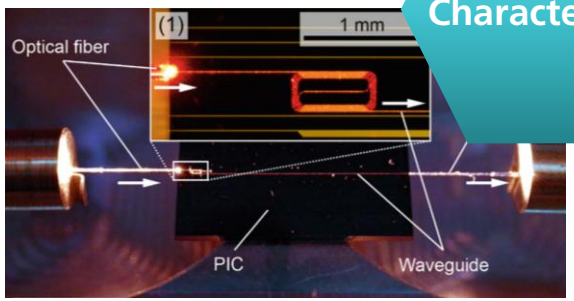


Design / Layout



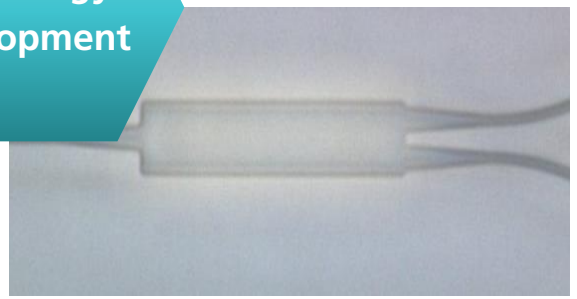
Simulation

Electronics & Photonics



Characterization

Technology Development



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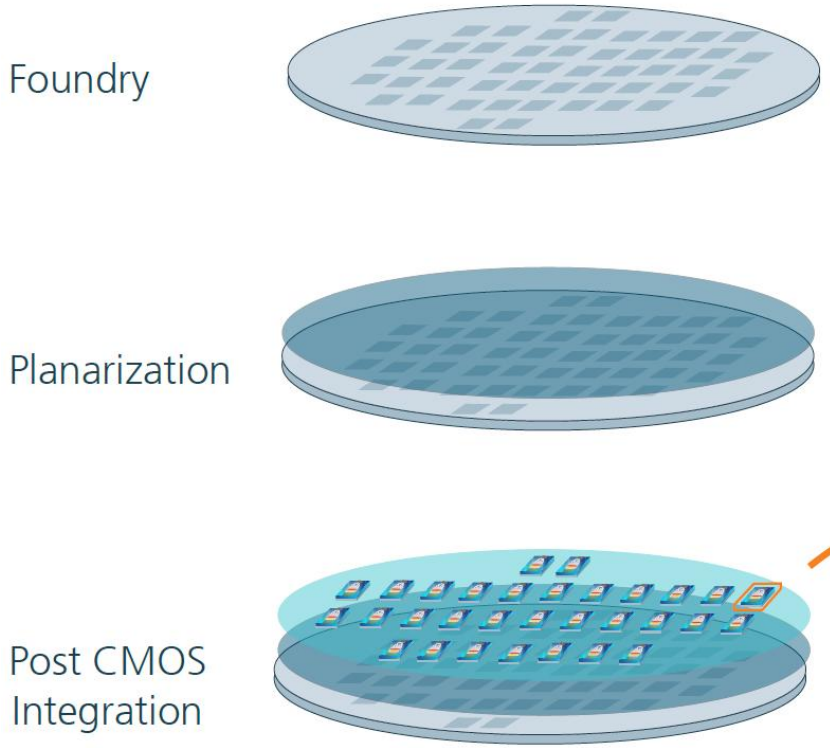
200 mm post-CMOS Photonic Platform

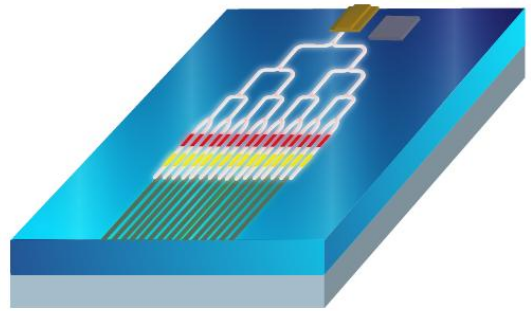
Post-CMOS Integration

- **CMOS compatible photonics: high bandwidth, compatibility with existing fabrication processes**
- **CMOS microelectronics: high integration density, low cost**
- **Post-CMOS Photonics: combining the CMOS compatible photonics with CMOS microelectronics.**
- **Various application are possible, i.e., communication, sensing, imaging, computing.**

[1]



Microscope image: Ring resonator integrated onto CMOS circuitry



Photonic layers (colored & white) and CMOS chip (grey)

[2] A. L. Schall-Giesecke. „Post-CMOS Photonic Integration“ Optics & Photonics News 6 (2025).

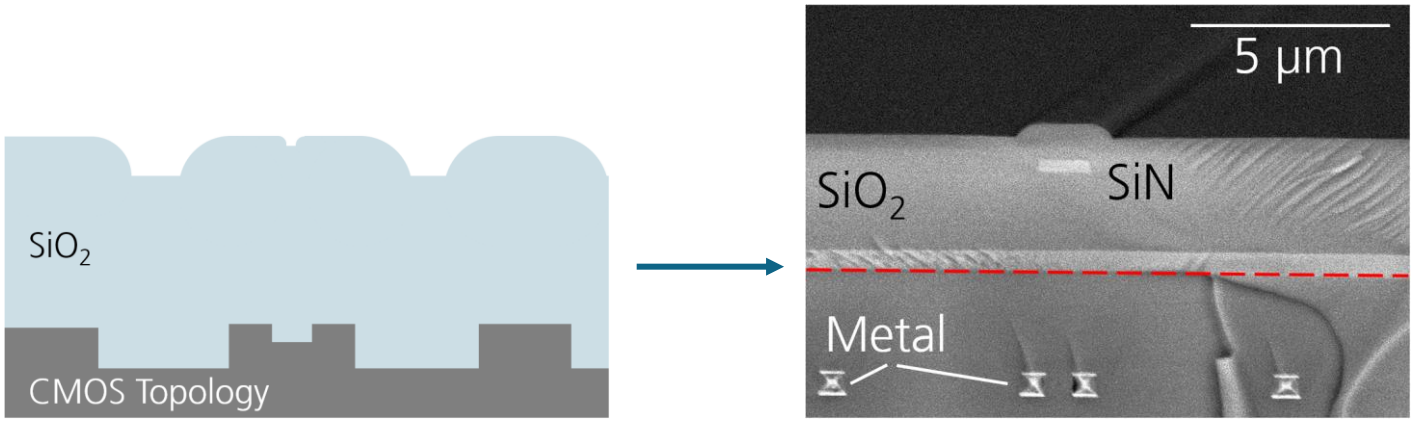
Fraunhofer IMS

Post-CMOS Integration
Planarization

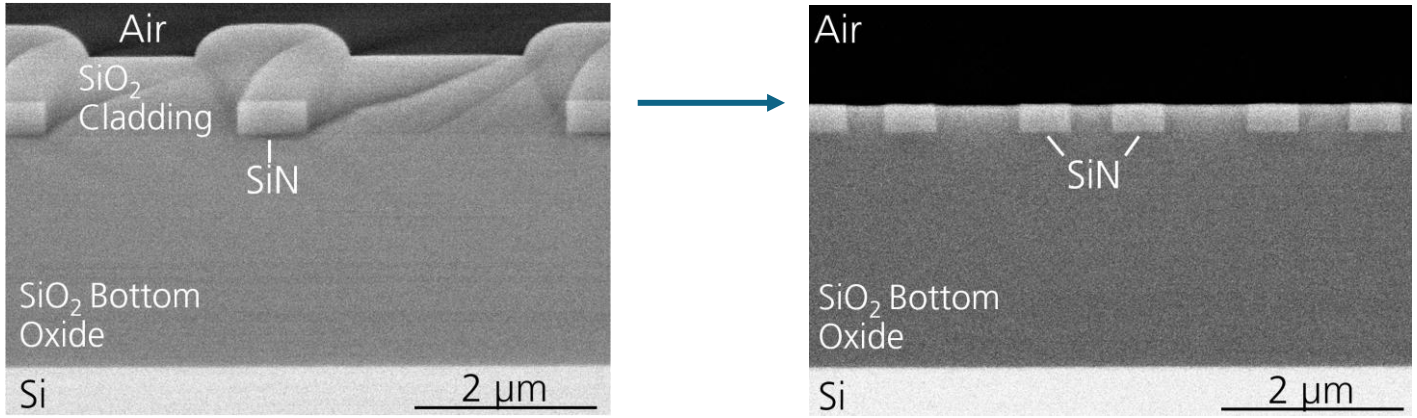
Chemical-Mechanical Polishing (CMP)

- Wafer-Scale
- Standard CMOS process
- CMP is used to
  - Flatten (CMOS) substrate (top SiO_2 layer) to allow for deposition of photonic layers
  - Make a flat interface on top of photonic layer for integration of:
    - Additional waveguide layers
    - Metal heaters/reflectors
    - 2D materials (e.g., graphene)
    - Atomic layer deposition of active materials
    - Polymer waveguides

Back end of line CMOS Planarization



Waveguide Planarization

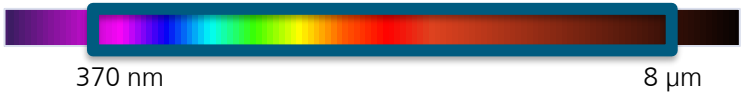


Technology Development

Waveguide Materials

Si_3N_4

Silicon nitride is a key material in integrated photonics.



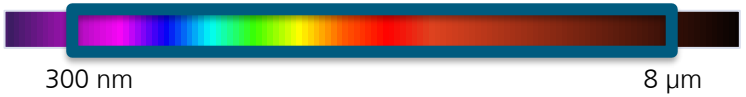
LPCVD
✓ Ultra-low propagation loss
✗ High film stress
✗ Not post-CMOS-compatible

PECVD
○ Low propagation loss
✓ Low film stress
✓ post-CMOS-compatible

Sputtering
✓ post-CMOS-compatible

Ta_2O_5

Tantalum pentoxide is an emerging material in integrated photonics.

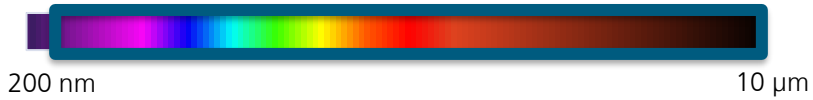


ALD
○ Low propagation loss
✓ Precise thickness control
✓ post-CMOS-compatible

CVD
✓ post-CMOS-compatible

AlN

Aluminum nitride is a wide-bandgap material commonly used for ultraviolet to mid-infrared photonics.



Sputtering
○ Low propagation loss
✓ high electro-optical coefficient
✓ post-CMOS-compatible

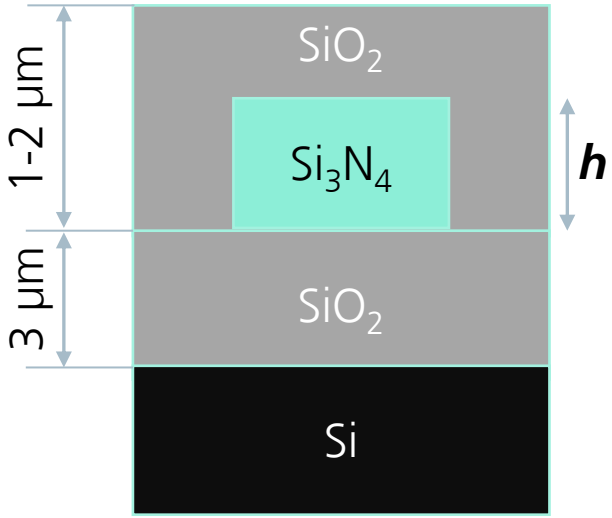
ALD
✓ post-CMOS-compatible

Waveguide and Material Types

[2]

High temperature

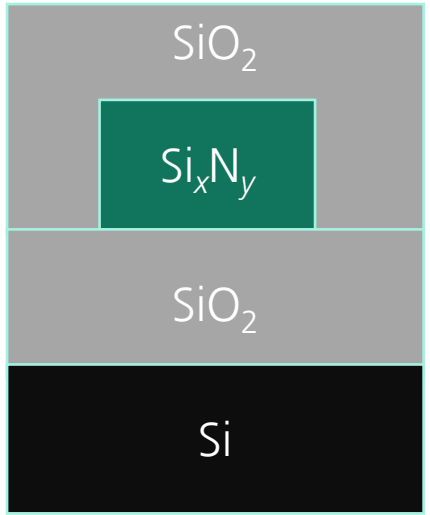
LPCVD



h = 0-360 nm

Post-CMOS for IR wavelengths

PECVD



h = 0-800 nm

Post-CMOS for Visible wavelengths

PE-VIS

h = 0-800 nm

Material optimized for visible wavelength range

Post-CMOS for thin waveguides

ALD

h = 0-200 nm

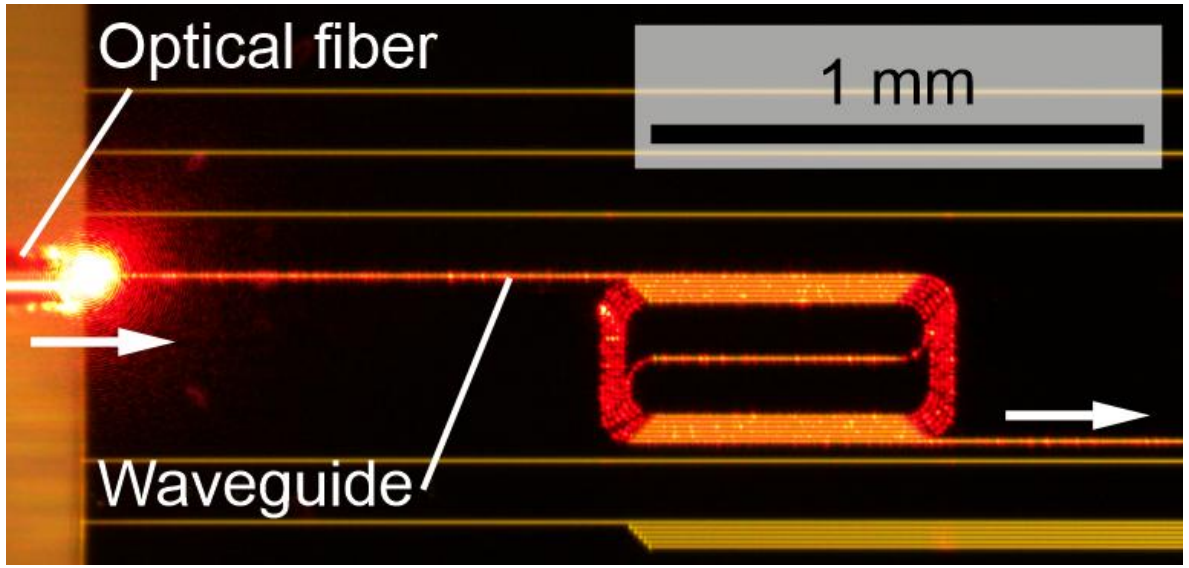
[2] Westhues *et al.* "Highly flexible dielectric platform for post-CMOS photonics," European Conference on Integrated Optics (ECIO) 2024, Aachen

Fraunhofer IMS

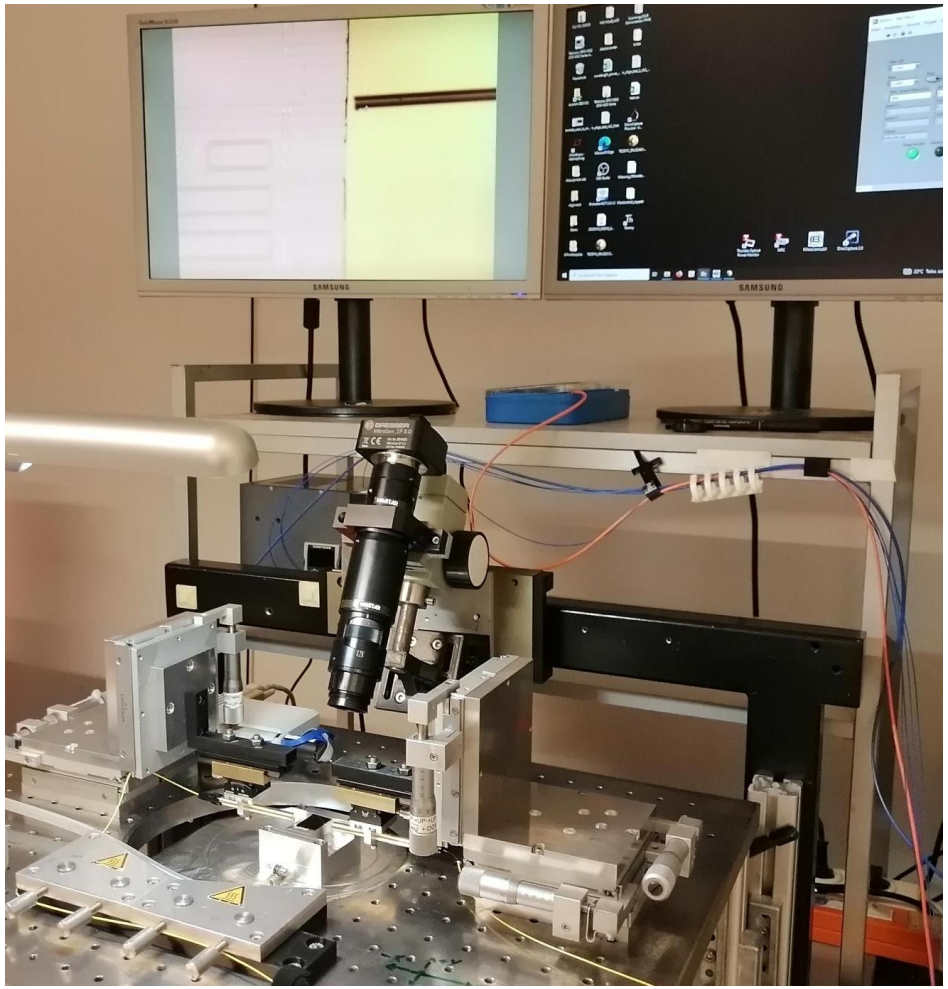
Semi-automated characterization setup for up to 200 mm wafers

- Optical and electro-optical characterization setup
- At λ = 400 nm, 630 nm, 785 nm, tunable laser 1490-1640 nm, supercontinuum laser from 400-1900 nm
- Significant upgrade of characterization equipment in 2026 and 2027 within APECS.

[2]



Side coupling of 630 nm light into PE-VIS chip



[2] Westhues *et al.* "Highly flexible dielectric platform for post-CMOS photonics," European Conference on Integrated Optics (ECIO) 2024, Aachen

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