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greener electronics
FD-SOI · NVM · 3D · RF · PMIC

# Webinar

## Exploring the Grenoble Semiconductor Ecosystem and the FAMES Pilot Line

*February 2nd, 2026*

CHIPNL Competence Centre

**Bruno Paing**, VP Europe & International Public Affairs – CEA-Leti (bruno.paing@cea.fr)

cea leti

# CEA-Leti

## Research & Technology Organization

*Grenoble, France*

# CEA-Leti mission & key figures

Created in **1967**, **CEA-Leti is located in Grenoble**, France

Benefits of a world-leading R&D organization:

**A commitment to long-term collaborations**
~2,000 experienced research engineers

**World-class technological platforms**
13,000m² cleanroom space (200 & 300 mm)

**Multidisciplinary applied research**
3,200 patents in portfolio

**Partnerships with industry**
300 industrial partners
75+ startups created

**Budget: 450M€** (85% from R&D contracts)

# At the heart of the French Alps
# Silicon Valley

APPLIED MATERIALS · Mentor A Siemens Business · Air Liquide · SCINTIL PHOTONICS · Aledia innovative displays · microoled · GETINGE FLUOPTICS · PIXYL · Device-ALab · KOELIS Advancing Prostate Care · LYNRED

Detection Technology · INSIDIX IMAGING TECHNOLOGY · MAG 4He alth · IMACTIS a GE HealthCare company · ARM

life.augmented · soitec · NXP · KALRAY · cea leti

ecential robotics · SteerLight · TRIXELL · intel · pyxalis

SYNOPSYS · NAVER · Hprobe · Mentor A Siemens Business · Lam RESEARCH · GREENWAVES TECHNOLOGIES · TELEDYNE e2V Everywhereyoulook · FUJIFILM FUJIFILM Electronic Materials Global · THALES · unity SC · TDK · SILVACO


Credit: kevin.s38

# CEA-Leti semiconductor platforms

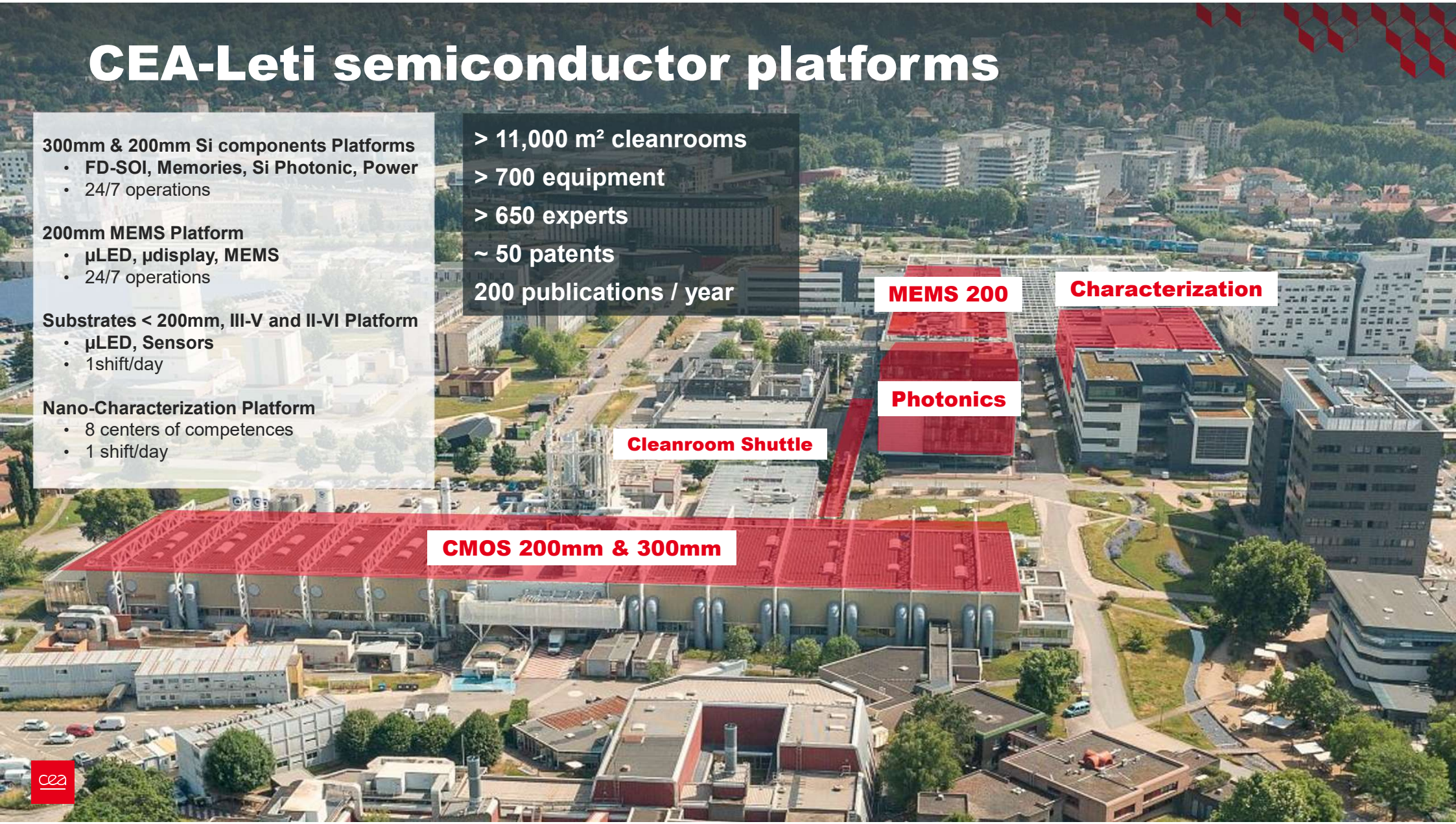
**300mm & 200mm Si components Platforms**
- **FD-SOI, Memories, Si Photonic, Power**
- 24/7 operations

**200mm MEMS Platform**
- **µLED, µdisplay, MEMS**
- 24/7 operations

**Substrates < 200mm, III-V and II-VI Platform**
- **µLED, Sensors**
- 1shift/day

**Nano-Characterization Platform**
- 8 centers of competences
- 1 shift/day

**> 11,000 m² cleanrooms**
**> 700 equipment**
**> 650 experts**
**~ 50 patents**
**200 publications / year**



cea leti

**700** state-of-the-art tools

**11,000 m²** cleanroom space

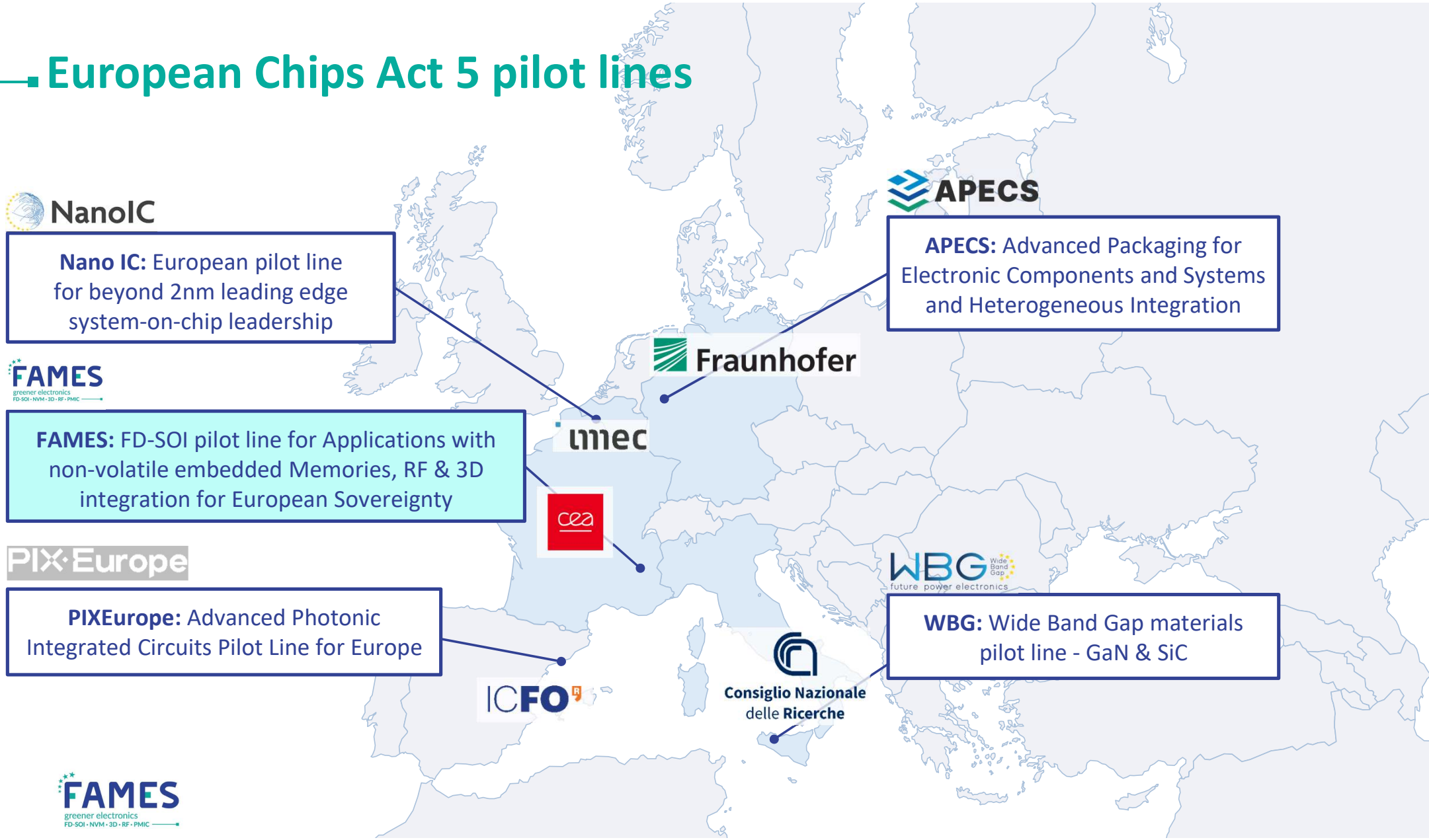
# More than Moore

# World-class facilities for your future needs

## Main Technology Baselines

| Wafer sizes (mm) | | | |
|---|---|---|---|
| | 300 | 1 | NW GAA / BEYOND CMOS |
| 200 | 300 | 2 | EMBEDDED MEMORIES |
| 200 | 300 | 3 | RF (active and passive devices) |
| 200 | 300 | 4 | Si PHOTONICS |
| 200 | 300 | 5 | µLED DISPLAY |
| | 300 | 6 | IMAGERS |
| | 200 | 7 | MEMS |
| 200 | 300 | 8 | POWER (Si, GaN, SiC) |
| 200 | 300 | 9 | 3D |
| 200 | 300 | 10 | SUBSTRATES |
| | 200 | 11 | II-VI and III-V |

# European Chips Act 5 pilot lines

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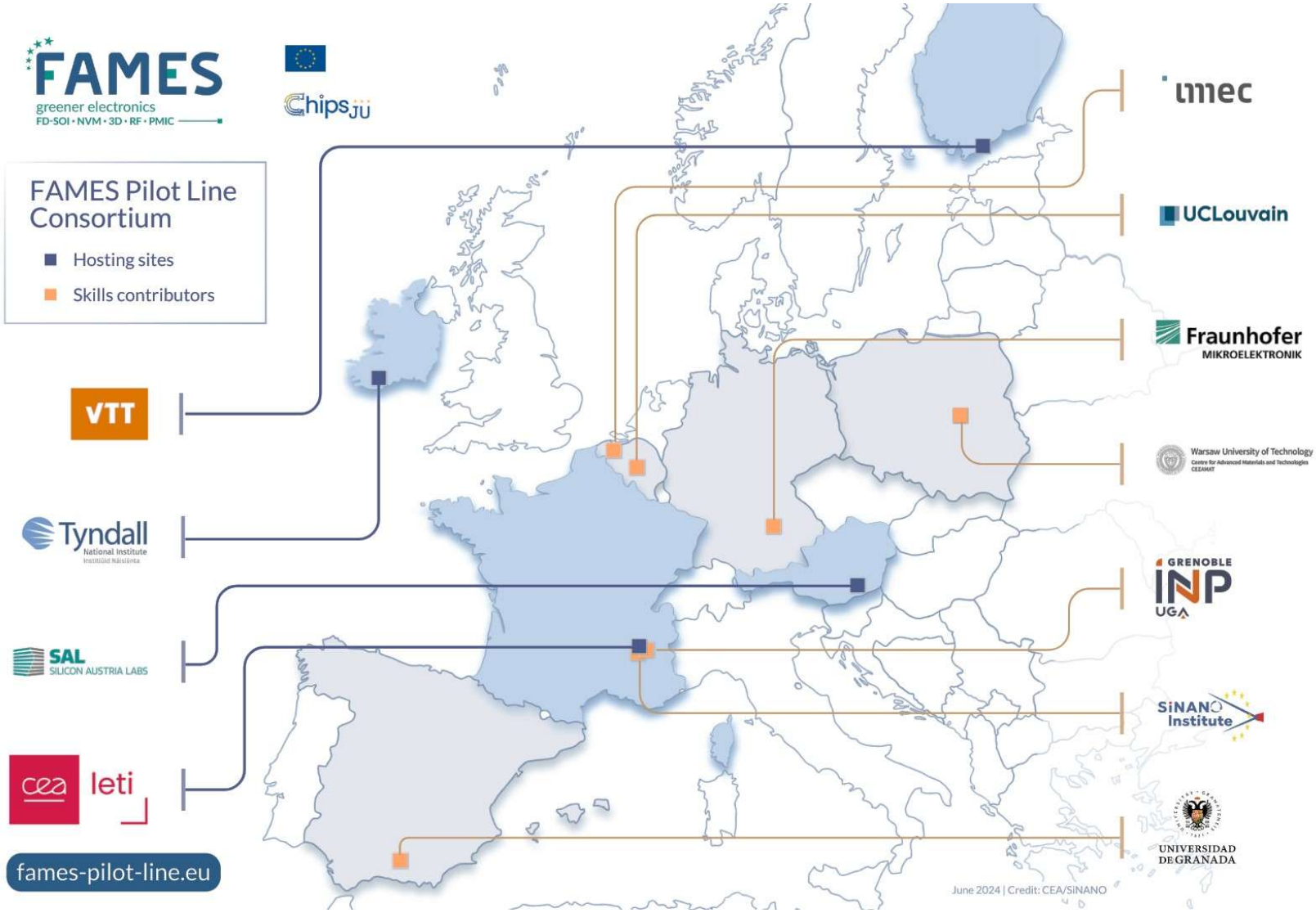
**Budget** : €830 M
- CAPEX: €382 M
- OPEX: €448 M

**Funding mechanisms**
- 50% Chips JU
- 50% Member States

**Dec. 2023 → Dec 2028**



# Aim of FAMES

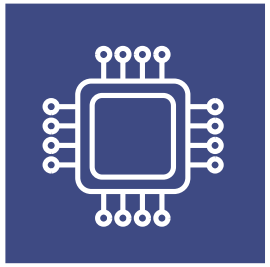
- A European semiconductor pilot line for advanced technologies
- With opportunities for disruptive chip architectures, performance improvements and significant energy savings
- Strengthening European leadership in advanced semiconductors and opening new economic opportunities for a wide spectrum of markets

Credits: Jayet/CEA

# Opening the pilot line to European stakeholders

## 44 letters of support

# FAMES Key Activities



**R&D**

**5 Technologies + an eco-innovation Program**

**Pilot line implementation**

**Cleanroom equipments**

**Open-access**

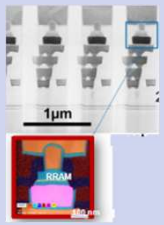
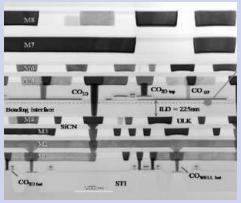
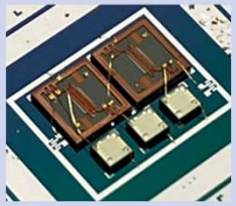
**Yearly Calls Spontaneous Requests**

**Training & education**

**Workshops, webinars and schools**

# FAMES Technology Portfolio

# FAMES technological offer

| FD-SOI | Embedded non-volatile memories | Radiofrequency components | 3D integration | Small inductors for DC-DC converters | Eco-innovation |
|---|---|---|---|---|---|
| 10 nm and 7 nm nodes<br>  | OxRAM, FeRAM, MRAM and FeFET<br>  | Switches, filters, and capacitors<br>  | Heterogeneous and sequential<br>  | Power management integrated circuits (PMIC)<br>  | Evaluate and reduce environmental footprint<br>Planetary boundaries<br>Environmental regulations |
| cea leti<br>imec<br>UCLouvain | cea leti<br>VTT imec<br>UCLouvain<br>Fraunhofer<br>UNIVERSIDAD DE GRANADA | cea leti<br>VTT<br>SAL SILICON AUSTRIA LABS | cea leti<br>Tyndall National Institute | cea leti<br>Tyndall National Institute | cea leti<br>imec cea list<br>UCLouvain |

**FD-SOI is the optimal PPAC-E (Power, Performance, Area, Cost, Environmental impact) trade-off for mixed-signals circuits**

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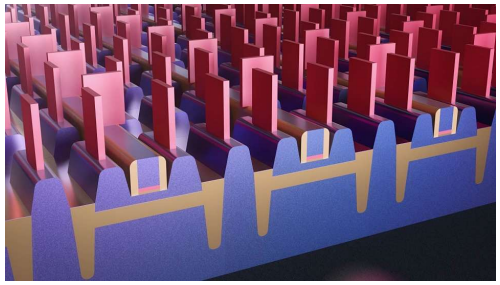
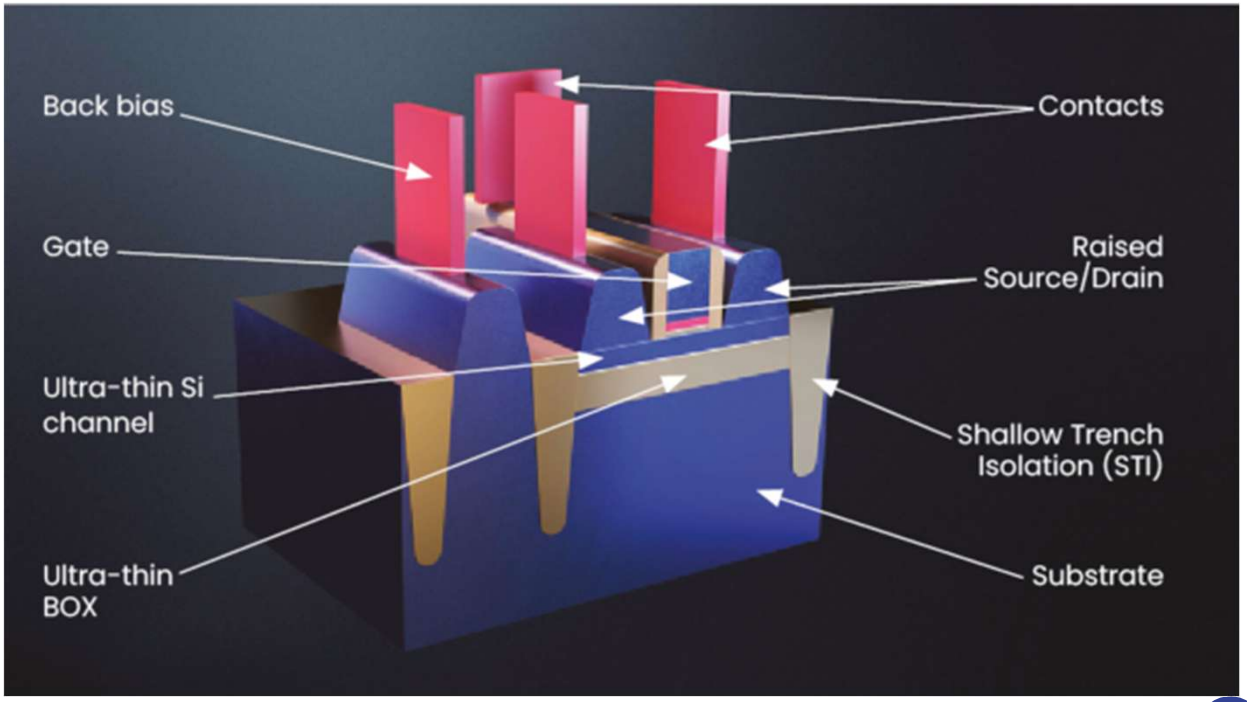
# FD-SOI advanced nodes (10 - 7nm)



**An innovative generation of chips with the best balance in Power, Performance, Area, Cost and Environment (PPAC-E) for highly energy efficient applications**

- Transistor density
- High-performance/low-power trade-off
- Radiation resistance
- Reduced current leakage
- Manufacturing costs

- Over **150 patents** filed by CEA-Leti

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# Radiation resistance, should we matter? Yes, we should…

BBC

## Bit flips: How cosmic rays grounded a fleet of aircraft


**Radiation from space that led to more than 6,000 Airbus aircraft needing emergency computer updates could become a growing problem as ever more microchips run our lives.**

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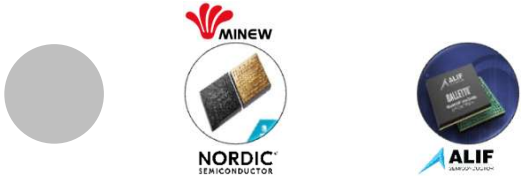
# More than 100 FD-SOI products on the market in 2025

## Wireless communication

### 5G Smartphones


*mmW Transceiver*

### Wi-Fi / Bluetooth LE Modules




*WIFI 7* | *Multiprotocol MPU* | *Audio MCU with BLE*

## Automotive

### Front-End Camera


*Image Processor*

### Thermal Camera


*LWIR Smart Sensor*

### Radar


*77-120 GHz SoC*

### Digital Cockpit


*Multi-media MCU*

### E-Powertrain


*32 bits MCU*

## Wearables

### Smartwatches


*Crossover MCU* | *GNSS*

### Smartglasses


*Audio Processor* | *Display Driver*

### Earphones


*Audio Processor*

## Embedded Computing

### Edge AI


*NPU* | *FPGA* | *USB Stick*

### Cameras


*Image Processors*

### Smart Speakers


*Audio Processor*

## Aerospace

### Satellites


*Transceiver* | *FPGA*

### Avionics


*MCU*

## Quantum

### Computing


*QPU*

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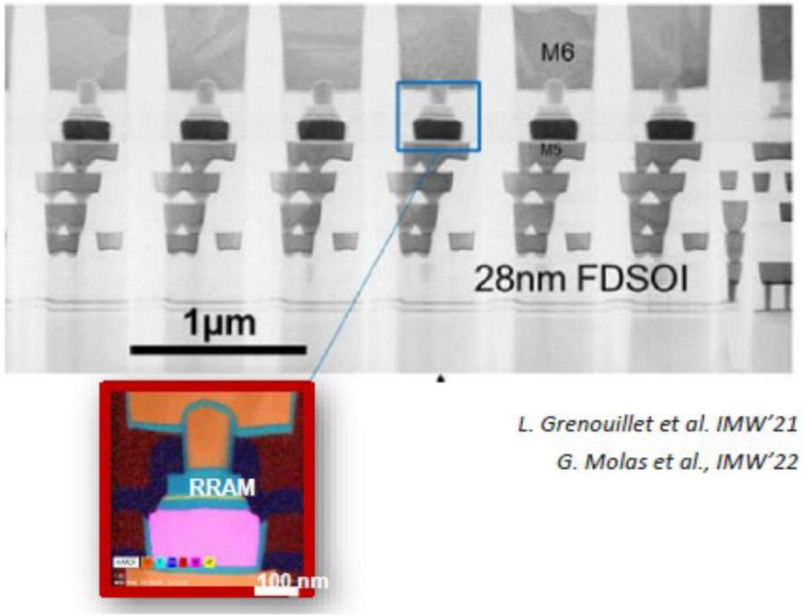
# Emerging Non-Volatile Memories embedded in the BEOL



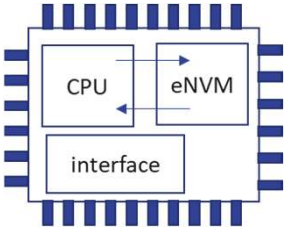

*L. Grenouillet et al. IMW'21*
*G. Molas et al., IMW'22*

**EMBEDDED** quicker access time and lower power compared to stand alone as they are on chip close to the logic

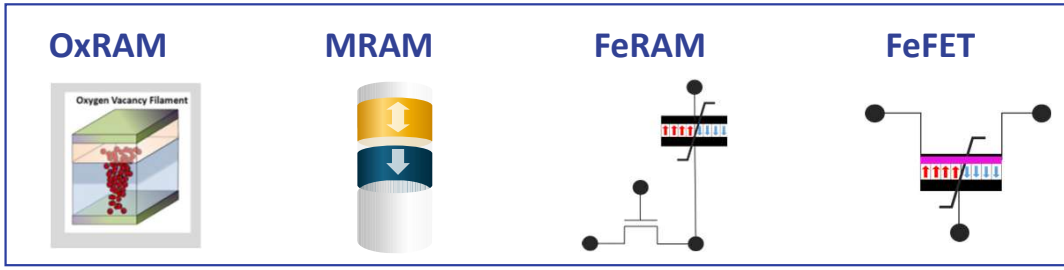
**NON VOLATILE** retaining data even when the power is off

**PERFORMANT** reprogrammable and erasable multiple times, faster to write compared to Flash memories

**LOW POWER** lower power consumption than external non volatile memories




**OxRAM** **MRAM** **FeRAM** **FeFET**

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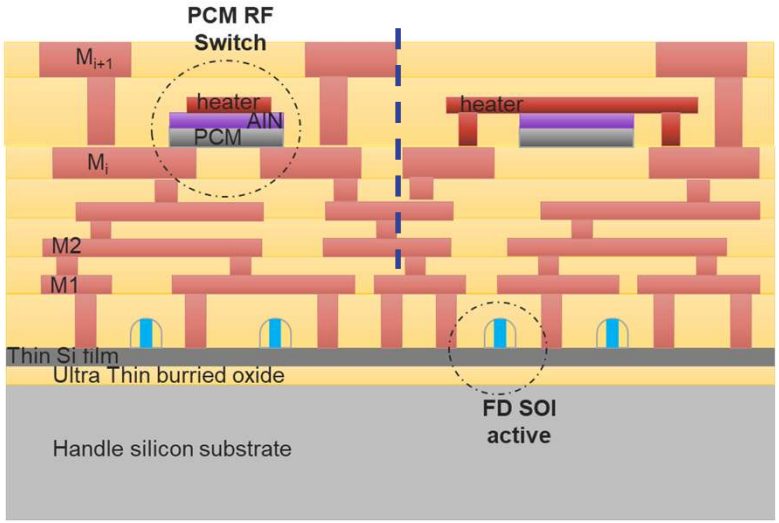
# RF components integrated in the BEOL

FD-SOI is well-suited for RF/analog and mixed signal circuits

- **Performance/power savings**
- **Covering a wide frequency range**
- **From a few GHz up to the D-band centered at 140 GHz**




FAMES → RF active and **passive components**, to enrich the FD-SOI CMOS technology offer and open new markets:

- **RF switches based on Phase Change Materials**
- **RF acoustic filters**
- **RF magnetic-based miniaturized circulators for >GHz bands**

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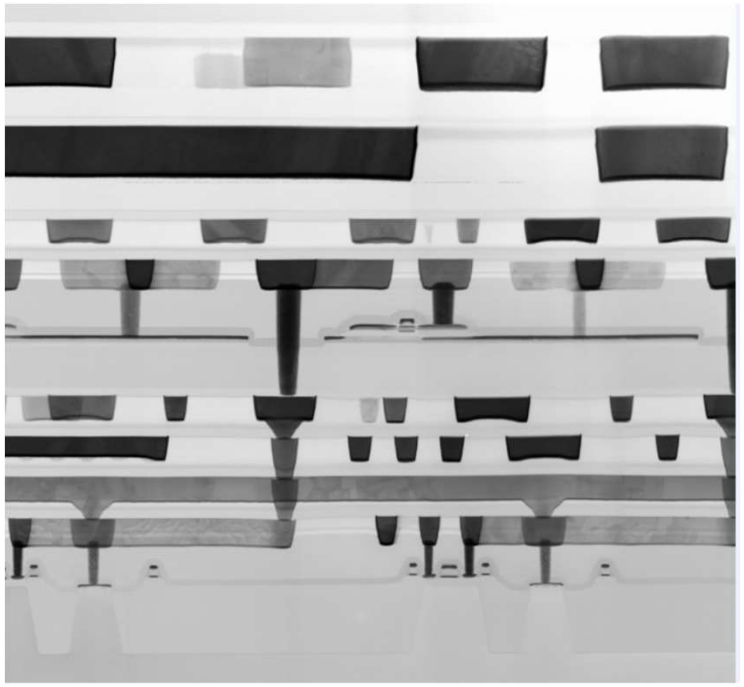
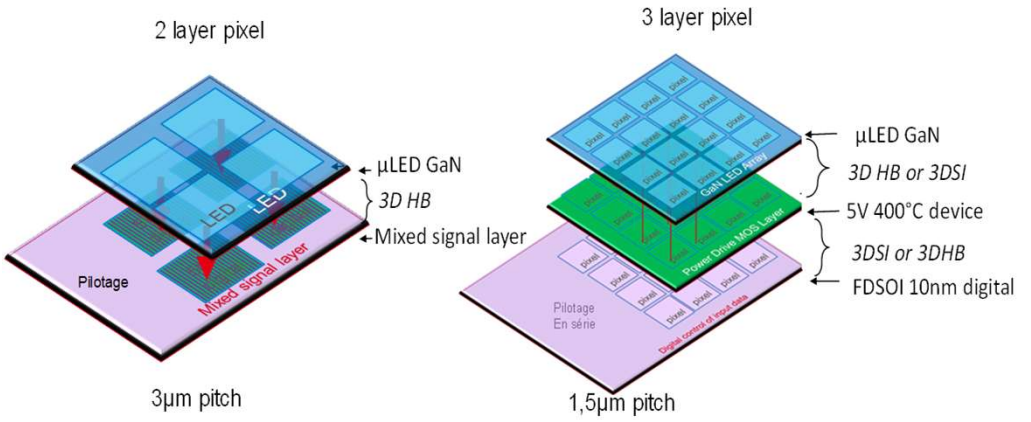
# 3D Sequential integration



"High Performance 2.5 V n&p 400 °C SOI MOSFETs: A Breakthrough for Versatile 3D Sequential Integration," D Bosch et al. IEDM 2025

## FAMES aims to enlarge FD-SOI heterogeneous co-integration with other devices using 3DSI to address new systems and markets

- Demonstrate 3D sequential integration with increasingly complex circuits;
- Evaluate opportunity of Smart and scaled 3tier-pixels with GaN µLED and RF applications

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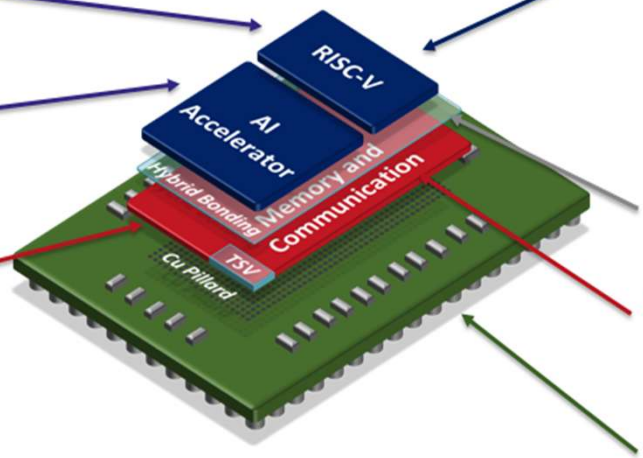
# Edge computing based on 3D hybrid bonding (HB) chiplet architecture

**Architecture**

- **Generic Computing with OpenHW**
- **Low power accelerator**
- **Chassis die** with peripherals, IOs, memory and communication infrastructure




**Technology**

- **Multi-chiplets:**
  - Advanced technology node
  - Heterogeneous (size, technology node, pitch)
  - Face down
  - No TSV
  - Full digital compute chiplet
- **Hybrid bonding:**
  - Die-to-wafer, Face-to-face
- **Base die:**
  - Mature technology node
  - TSVs for power delivery and IOs
  - Face-up
- **Package**

**Novel 3D approach developed by FAMES: Chiplet architecture with very low latency**

- TSV : Back-Side Mid-BEOL TSVs
- Cu/SiO2 HB : 5 µm pitch
- Front-Side and Back-Side RDLs

→ **To increase interconnect density by a factor of up to 100**

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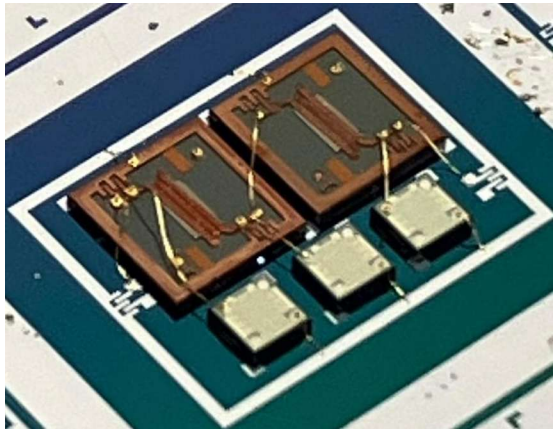
# Integrated Magnetics and PMIC for DC-DC power conversion



## Power management integration in Systems-on-Chip

- Power converters densely co-integrated with digital or RF loading blocks
- Solutions to improve **power delivery** in chiplet architectures
- **Integration of passive components close to SOC**
- Design and fabrication of **integrated magnetics for inductive passive** components

## FAMES will provide solutions to improve power delivery by integrating passive components into SOC

- Design and fabrication of integrated magnetics for inductive passive components
- Collective assembly of passives by Micro Transfer Printing (MTP)
- Performance assessments via a functional technology demonstrator that integrates an inductance-based DC-DC power converter, for granular power delivery

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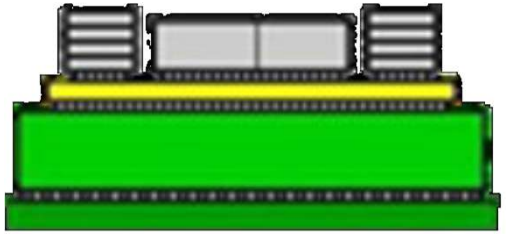
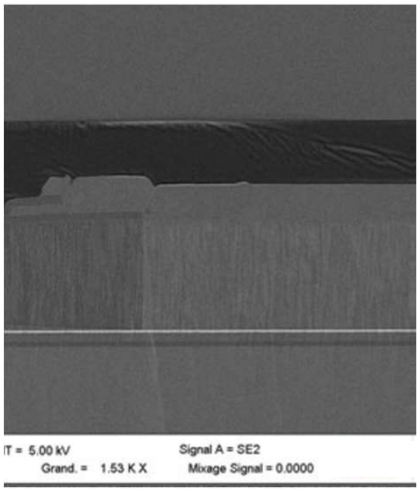
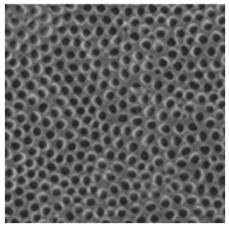
# Power conversion: 3D caps



*Hybrid integration*




*Higher surface capacitors*



*High A/R MIM*

Hybrid integration of high density capacitors and CMOS power conversion stages on 300mm wafers for advanced 6G systems and HPC applications

- Very high density capacitors:
  - Specific ALD method developed for a MIM deposition with aggressive aspect ratios
  - TiN bottom and top electrodes
  - Si oxide and/or alumina for dielectrics

**A game-changer for power signal management**

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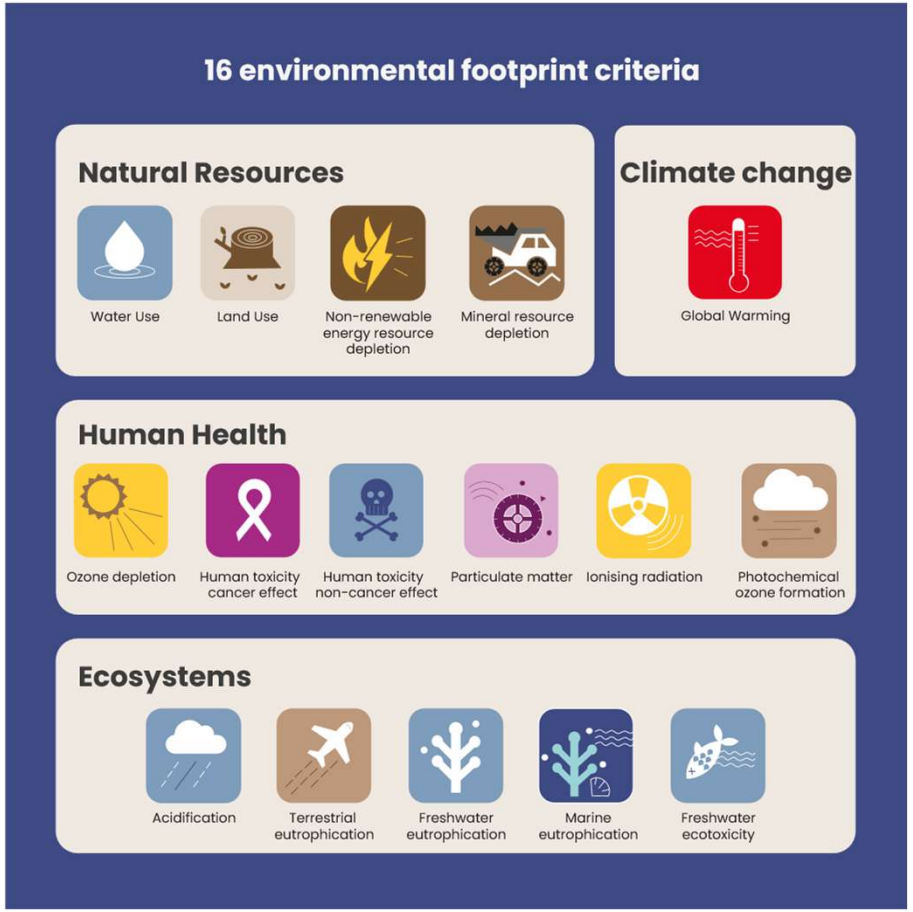
# FAMES Eco Innovation Offer

**Eco-innovation for more sustainable electronics**
Reducing the impacts of electronics through R&D

- The development and implementation **of lifecycle analysis (LCA)**
- The validation of eco-innovative solutions in a production-like environment
- The development of technologies and end-to-end systems to meet specific environmental criteria for identified use cases.

## 16 environmental footprint criteria

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# New facility and Pilot Line tool capability in Europe


Credit: P Jayet / CEA

**January 30, 2026**

**New cleanroom at CEA-Leti**
**2000m² double basement state of the art facility**

**Procurement of 100+ pieces of equipment planned by the Pilot Line on 4 hosting sites**

- France
- Finland
- Ireland
- Austria

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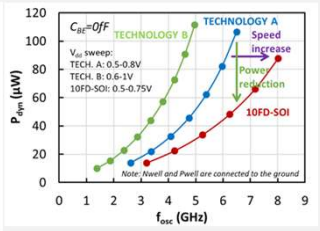
# FAMES year 1 results highlights

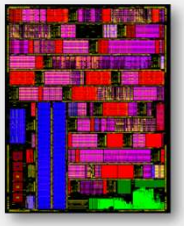
## Infrastructure and procurement

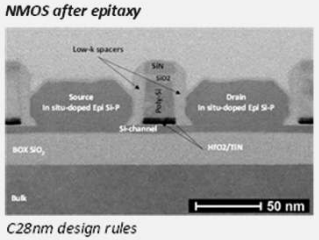
- New cleanroom at CEA-Leti planned for delivery in 2025
- 24 pieces of equipment installed /15 ready for production
- **Official inauguration on October 17th, 2025**


## FD-SOI

- FD-SOI 10nm process assumptions ready for perf. evaluation
- First FD-SOI 10nm DRM and first GDS ready for tapeout
- Key process modules and FD-SOI10 architecture developed on relaxed pitch



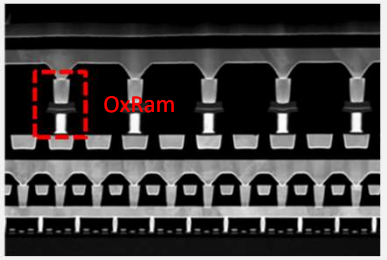



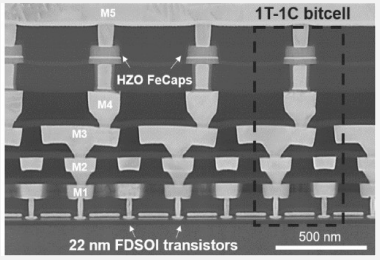


C28nm design rules

## eNVM

- OxRAM 0.05 µm bit-cell tested
- FeRAM test vehicle characterized: **best state of the art** presented at IEDM2024
- Wafer scale MoS2 growth demonstrated

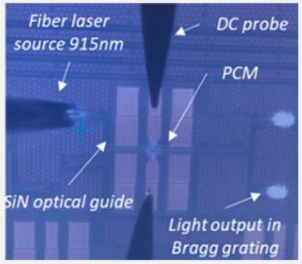


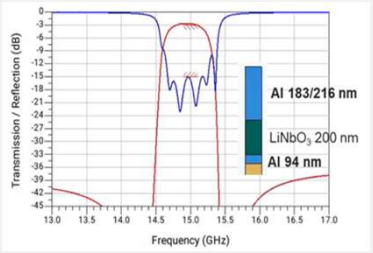



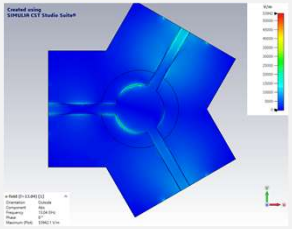
# FAMES year 1 results highlights

## RF components

- PCM RF switch with optical actuation (**world first**)
- FR3 $LiNbO_3$ filter design @15GHz
- FR3 and FR2-1 bands circulator design



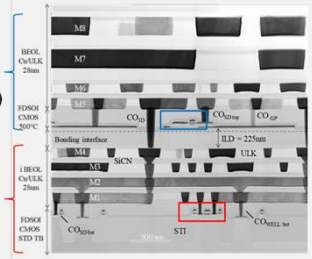



## 3D integration

- High density integrations (<5nm alignment) with sequential process
- Digital/RF 3D integration tested – cross talk analysis
- TSV process development for hybrid bonding integration

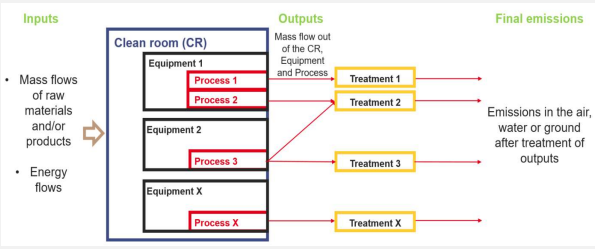
- Process flow & CMOS stack
  - FDSOI 28nm CMOS platform
  - 4 metal level Cu/ULK (28nm)
  - Ultra thin Inter Layer Dielectric (ILD)
  - Top channel and doped poly GP by bonding
  - FDSOI CMOS at 500°C
  - 3D contacts W/H = 100/450nm
  - 6 metal level Cu/ULK (28nm)



*J. Lugo-Alvarez et al, VLSI 2024*

## Sustainability and environmental impact

- Life Cycle Assessment methodology
- E-score to introduce environmental KPI (PPAC-**E**)
- Cleanroom data collection platform

# Accessing the FAMES Pilot Line

# The FAMES Pilot Line is open to all types of Users

LARGE COMPANIES

SMEs

START-UPs

RESEARCH COMMUNITY

Design Houses
Fabless
Foundries
Integrated Device Manufacturers
Material and Tool Suppliers
Universities
Research Centers

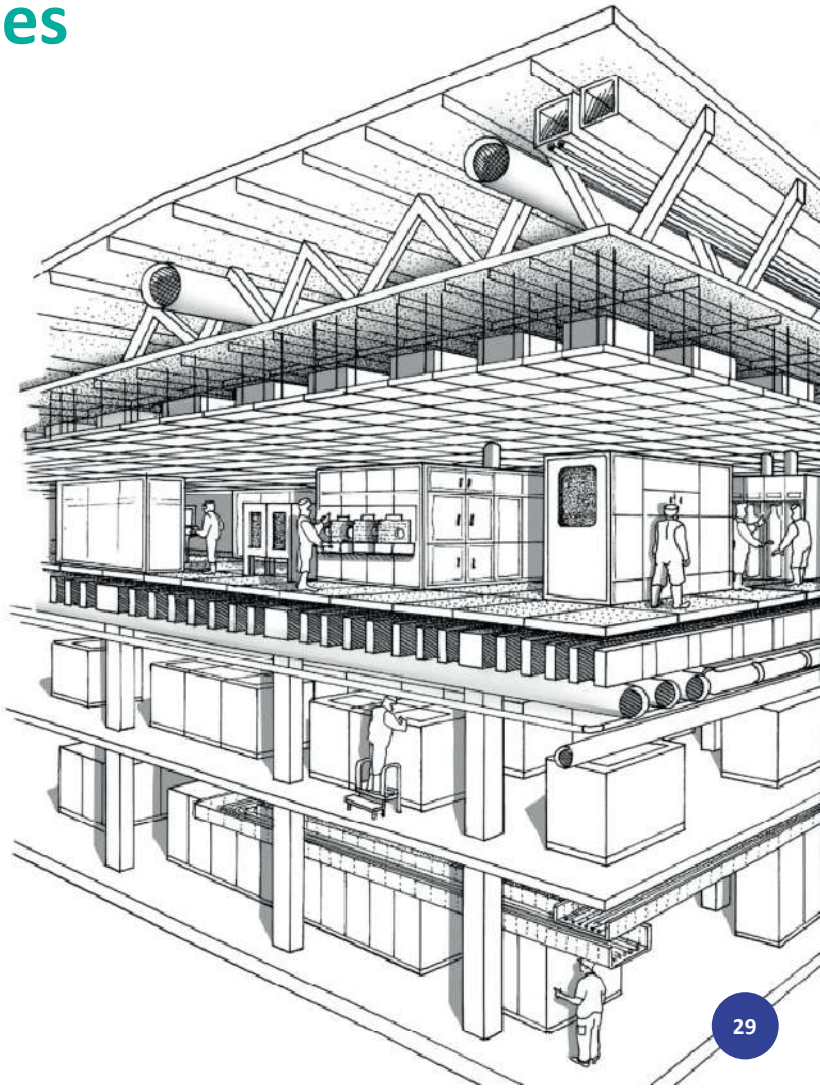
# FAMES European open-access Pilot Line for advanced semiconductor technologies

Aim: Facilitate the adoption of FAMES Technologies to strengthen the European semiconductor ecosystem

To gain access to:

- Two types of PDKs (multi-project wafer or IC design assessment)
- The FAMES technologies (FD-SOI advanced nodes, embedded non-volatile memories, RF components, 3D integration options, PMIC) for performance evaluation
- Specific process steps, modules, integration flows, and demonstrator results
- Education and training on the FAMES technologies

as they become available



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# The FAMES Pilot Line's synergy with the Research Community

RESEARCH COMMUNITY

- Leverage PDKs to create innovative IPs leading to new fabless start-ups
- Collaborate with FAMES partners and provide feedback on first PDK releases
- Define disruptive chip architectures for new ICs
- Get young researchers trained on FD-SOI and FAMES technologies to increase the emergence of EU-made breakthrough chips

# Two ways for Users to access the FAMES Pilot Line

Yearly Open-Access Calls
March to May

fames-pilot-line.eu

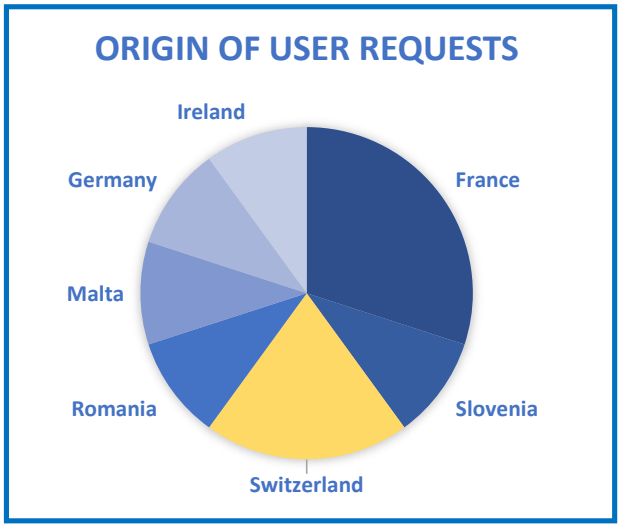
Spontaneous Requests
All year round

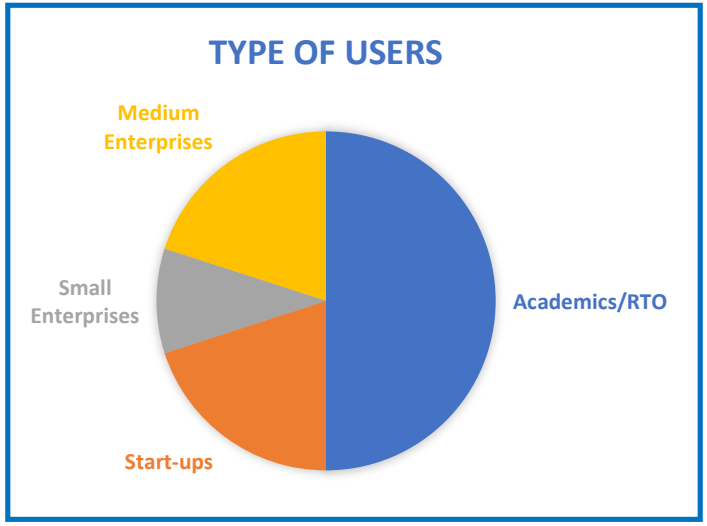
fames-pilot-line.eu

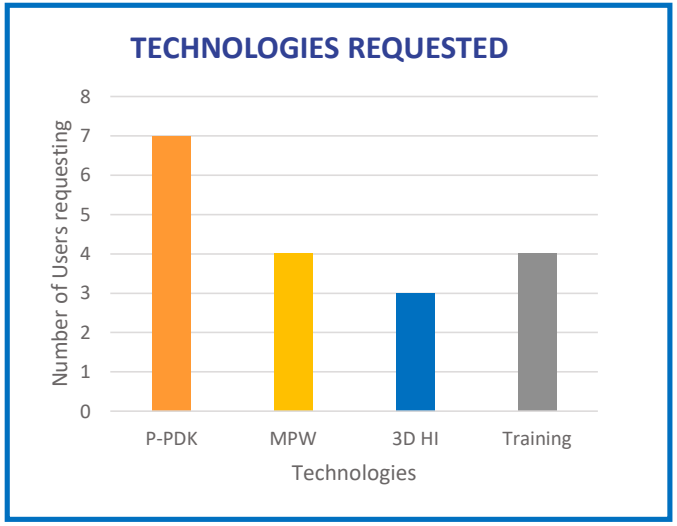
Competence centers and Design Platforms

# User Requests received / first FAMES Open-Access Call (2025)

- **Domains:** Telecommunications, Quantum, Cognitive and Edge AI, Power Management, Chip Design Tools, Teaching



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# FAMES 2026
# Open-Access Call Launch

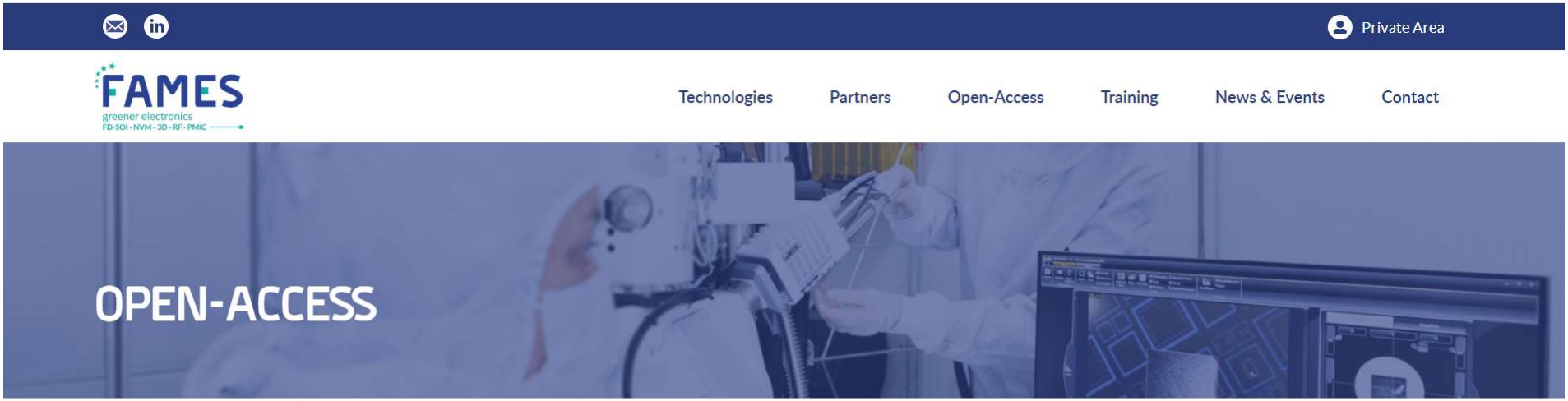
The FAMES Pilot Line

fames-pilot-line.eu

When March 9, 2026

Where Full Remote Event

# Website: Open-Access page




## FAMES Pilot Line

The FAMES Pilot Line offers European semiconductor stakeholders from industry, research, and academia **access to a unique slate of advanced semiconductor technologies**, chip design, testing, demonstrators and manufacturing capabilities.

This initiative aligns with the EU Chips Act to bolster the EU's semiconductor industry and support European technological sovereignty. Collaboration with other pilot lines in Europe will help build a tightly interconnected European chip ecosystem.

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https://fames-pilot-line.eu/open-access/

# Follow the FAMES Pilot Line on LinkedIn!

@fames-pilot-line

# FAMES

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(2023 – 2028)

# Sponsors

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R.E.S.O.L.V.E

ENERGY EFFICIENCY GAIN
×1,000
by 2032

# RESOLVE Initiative

## Towards Chips Act 2


**R**educing
**E**nergy consumption for
**SO**vereignty and
**L**eadership in
**V**alue-added
**E**lectronics products


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